

PROGRAM AT A GLANCE



Tuesday, July 2nd	
<i>Amphitheater 1</i>	
09:00-10:30	Tutorial – Machine Learning for Design Automation
10:30-11:00	Coffee Break
11:00-12:30	Tutorial – Tackling Signal Integrity Challenges in Interposer and 3DIC Applications with Ansys RaptorX
12:30-13:30	Lunch
13:30-15:00	Tutorial – Exploring Radiation Effects for Reconfigurable SoCs in Space and Particle Accelerators
15:00-15:30	Coffee Break
15:30-17:00	Tutorial – Integrating Multiple Knowledge-based Automation Methodologies into the A/MS IC Design Flow
20:30-22:00	Welcome Reception

Wednesday, July 3rd		
	<i>Amphitheater 1</i>	<i>Amphitheater 2</i>
08:30-09:00	Opening Session	
09:00-10:00	Plenary Talk – <i>Prof. Yusuf Leblebici</i> “Designing Some of the Most Influential Hardware in Human History: Our Collective Responsibilities”	
10:00-10:30	Coffee Break	
10:30-12:10	Automated Circuit Design	<i>Special Session</i> Advances & Future Trends in Electronic Circuits & Systems with Emerging Devices
12:10-13:20	Lunch	
13:20-13:50	CEDA Presentation	
13:50-15:30	EDA Competition I	Cutting-edge Technologies for Automotive and Space
15:30-16:00	Coffee Break	
16:00-17:00	Innovations in Hardware Security I	Machine Learning for Modeling

Thursday, July 4th		
	<i>Amphitheater 1</i>	<i>Amphitheater 2</i>
08:30-09:30	Plenary Talk – Prof. Georges Gielen “Designing Analog Integrated Circuits: Designers, Synthesis or Generative AI?”	
09:30-10:30	EDA Competition II	
10:30-11:00	Coffee Break	
11:00-12:00	Sponsor Presentations	
12:00-13:40	Lunch and Job Fair	
13:40-15:00	Automating Layout and Technology Migration	Advanced Circuit Design I
15:00-15:30	Coffee Break	
15:30-16:30	EDA and the Human Factor	<i>Special Session</i> Safety and Security in Modern System-on-Chip (SoC)
20:30-22:00	Gala Dinner	

		Friday, July 5th	
		<i>Amphitheater 1</i>	<i>Amphitheater 2</i>
09:30-10:30		Novel Device Modeling and Characterization	Advanced Circuit Design II
10:30-11:00		Coffee Break	
11:00-12:40		Machine Learning for Design	IC Design Contest
12:40-13:50		Lunch	
13:50-14:50		Advanced Circuit Modeling	Innovations in Hardware Security II
14:50-15:20		Coffee Break	
15:20-16:20		Dealing with Reliability	Dealing with Verification
16:20-16:50		Award Ceremony and Closing	