SMACD 2025

Istanbul-TURKIYE

"where circuits come alive"

21th International Conference on Synthesis, Modeling, Analysis and Simulation Methods, and Application to Circuit Design

CONFERENCE PROGRAM

7-10 July 2025,

Istanbul Bilgi University,

Santral Istanbul Campus Istanbul, TURKIYE

DAY-1

Monday

07.07.2025 | 08:00 - 17:30

8:00 – 9:00: REGISTRATION

Location: Entrance (E3)

09:00 – 10:30 : TUTORIAL-I

Room: Ömer Cerid

SoC Verification – Introduction, Agile Management, and Advanced Techniques

09:00 - 09:30: Talk 1: Introduction to Verification
Presenter: Melike ATAY KARABALKAN (Engineering Manager, Electra-IC, İstanbul Türkiye)

9:30 - 10:00: Talk 2:Your Gateway to Faster, Smarter SoC Verification with Agile Project Management
Presenter: Melike ATAY KARABALKAN (Engineering Manager, Electra-IC, İstanbul Türkiye)

10:00 - 10:30: Talk 3: Simplifying Complex SoC Verification for Modern Engineers
Presenter: Merve EYUBOĞLU (Digital Design & Verification Engineer, Electra-IC, İstanbul Türkiye)

10:30 – 11:00 : COFFEE BREAK

11:00 – 12:30: TUTORIAL-II

Room: Ömer Cerid

RISC-V & Formal Verification – Emerging Approaches and Practical Insights

11:00:11:45: Talk 1: RISC-V Verification: Recent Approaches in Chip Design Verification
Presenter: Elif Betül Şen Özen (ANKASYS, Istanbul, Türkiye)

11:45-12:30: Talk 2: Formal Verification: An Introduction and Challenges in Practice
Presenter: Yusuf Eren (ANKASYS, İstanbul, Türkiye)

12:30 – 14:00 : LUNCH BREAK

14:00 – 15:30 : TUTORIAL-III

Room: Ömer Cerid

ML Accelerators on FPGAs – A Journey from Manual Design to AI-Assisted Workflows

Rashed Al Amin, PhD (University of Siegen, Germany)

15:30 – 16:00 : COFFEE BREAK

16:00 – 17:30 : TUTORIAL-IV

Room: Ömer Cerid

Power Management ICs for Automotive & Battery Systems

Kemal Ozanoğlu, PhD (ATEK MIDAS, Istanbul,Türkiye)

18:00 – 20:00: WELCOME RECEPTION

Location: KAYIKHANE

DAY-2

Tuesday

08.07.2025 | 08:00 - 17:30

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8:30 – 9:00 : OPENING CEREMONY

Room: Ömer Cerid

09:00 – 10:00 : KEYNOTE TALK

Room: Ömer Cerid
Chair: Okan Zafer Batur

Analog In-Memory Computing for Deep Learning Acceleration

İrem Boybat, Research Scientist, IBM Research Europe,Zurich, Switzerland

10:00 – 10:30 : COMPANY SESSION

10:30 – 11:00 : COFFEE BREAK

11:00 – 12:40 : SESSION-I

Regular Session-1: Modeling Techniques for Devices, Circuits, and Interconnects

Room: Ömer Cerid, Chair: Nestor Evmorfopoulos

11:00 - 11:20: Circuit-Level Modeling and Simulation of Read Disturbance Phenomena: RowHammer and RowPress
Eda Demirel, Engin Afacan, and Günhan Dündar

11:20 - 11:40: FET Modeling with Deep Neural Networks and GAN-Augmented Small Measurement Dataset
Milad Bafarassat, Melik Yazici, and Korkut Kaan Tokgoz

11:40 - 12:00: Characterization of Inter-Chip Interconnects Using Piecewise Effective Capacitance
Nilotpal Sarma and Anand Bulusu

12:00 - 12:20: Efficient Parameter Reduction for Statistical Behavioral Modeling
Jan Rödel, Carna Zivkovic, Neha Chavan and Christoph Grimm

12:20 - 12:40: CAD Modeling of a Wafer-level Packaging GaN Transistors for Electrothermal Simulation Using the Finite Element Method
Mohamed Belguith, Sonia Eloued, Moncef Kadi, Jaleleddine, Ben Hadj Slama, and Mahmoud Hamouda

Regular Session-2: Advances in FPGA-Based Computing and Applications

Room: Haliç, Chair: Sheldon Tan

11:00 - 11:20: Hardware-Software Co-Design for Resource Efficient Gesture Classification System for FPGAs
Rashed Al Amin and Roman Obermaisser

11:20 - 11:40: Investigation of Reconfigurable CORDIC Modes and Efficiency
Hisham Elrefai, Wafaa Sayed, Ahmed Radwan and Lobna Said

11:40 - 12:00: A Cost-Efficient Implementation of an SSVEP-Based Brain-Controlled Robotic Arm System
Hongliang Chen and Weiwei Shi

12:00 - 12:20: Verification of RISC-V R-type Instructions Using A Custom Cocotb Based Approach
Şennur Güney and İhsan Çiçek

12:20 - 12:40: FPGA-based Neural Network for Arabic and English Handwritten Digit Recognition
Abdulrahman Elsadiq, Hisham Elrefai and Lobna Said

12:40 – 14:00 : LUNCH BREAK

14:00 – 15:20 : SESSION-II

IC Design Contest Session

Room: Ömer Cerid, Chairs: Burcu Erkmen and İhsan Çiçek

14:00 - 14:20: A Linear LN-TIA with T-network Feedback Using High Value Gate Controlled PMOS Resistors
Hakan Çetinkaya and Yasin Talay

14:20 - 14:40: An Energy-Efficient Analog Integrated Neural Network for Cirrhosis Patient Survival Prediction
Konstantinos Cheliotis, Vassilis Alimisis, Vasileios Moustakas, Zisis Foufas, Anna Mylona and Paul P. Sotiriadis

14:40 - 15:00: Low Voltage Bandgap Reference using Intelligent Layout Generators in 22 nm FDSOI CMOS
Adilet Dossanov, Zhaoqun Guo, Uwe Eichler, Benjamin Prautsch and Vadim Issakov

15:00 - 15:20: A Novel 10-18 GHz Current-Reuse Distributed Cascode LNA Design
Yavuzhan Yavuz and Mustafa Berke Yelten

Regular Session-3: Advances in RF and Microwave Circuit Design

Room: Haliç, Chair: Korkut Kaan Tokgöz

14:00 - 14:20: A Low-Power Charge-Pump PLL for Sub-6 GHz 5G and IoT Wireless Communication Systems
Mert Korkut, Tugba Haykır Ergin and Huseyin Arda Ulku

14:20 - 14:40: A large tuning-range LC-VCO Design for Mixer-First Type Receivers
Emirhan Dilekoğlu and Mustafa Berke Yelten

14:40 - 15:00: Design of Ultra Wideband Power Divider/Combiner and Comparison on Results of Measurement and Simulation based on EM Solver Methods
Engin Çağdaş, Hakan Çetinkaya, Oğuzhan Kızılbey and Metin Yazgı

15:00 - 15:20: A Compact Flexible High-bandwidth Meander Line Patch Antenna for IoT Applications
Mehmet Selim Mamati, Şeref Keser and Mohammad Alsunaidi

15:20 – 15:50 : COFFEE BREAK

15:50 – 17:20 : SESSION-III

EDA Competition Session-1

Room: Ömer Cerid, Chair: Revna Acar Vural and Baykal Sarıoğlu

15:50 - 16:20: Co-Simulation for Automated Optimization of Integrated Cryogenic Qubit Electronics
Pau Dietz Romero, Caner Toprak, Lammert Duipmans, Stefan van Waasen and Lotte Geck

16:20 - 16:50: An LLM-assisted Analog IC Design Tool with Automatic Topology Selection and Circuit Sizing
Anh Nguyen and Chien-Nan Jimmy Liu

16:50 - 17:20: A Scalable Authentication Scheme for Detecting Unauthorized Dice in A Multi-Die IC
Zheng-Hao Wang, Shi-Yu Huang and Chi-Kang Chen

Special Session-1: Novel Circuit Techniques and Design Methodologies for Accuracy Improvement of Digital-to-Analog and Analog-to-Digital Converters

Room: Haliç, Chair: Francesco Gagliardi and Kemal Ozanoğlu

15:50 - 16:10: High-speed, low-power comparators utilizing a self-cascode configuration and a dynamically biased preamplifier technique
Mohammad Bayazi and Renato Negra

16:10 - 16:30: Combining Machine Learning and Optimization Techniques for the High-Level Design of Sigma-Delta Modulators
Gustavo Liñán-Cembrano and Jose M. de la Rosa

16:30 - 16:50: A Side-Channel Attack-Resilient Single-Slope ADC for Image Sensor Applications
Ceyda Korpe, Kareem Ahmad, Ece Ozturk, Kanishk Tihaiya, Ryanh Tran, Hyunsoo Yang, Junbin Yang, Günhan Dündar, Vincent Mooney and Kemal Ozanoglu

16:50 - 17:10: Sorting Errors Effects on Optimal Combination Algorithms for Digital-to-Analog Converters
Francesco Gagliardi, Massimo Piotto, Paolo Bruschi and Michele Dei

17:30 – 18:30 SOCIAL EVENT

DAY-3

Wednesday

09.07.2025 | 08:00 - 17:30

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09:00 – 10:00 : KEYNOTE TALK

Room: Ömer Cerid
Chair: Engin Afacan

EKV model for the design of Cryo-CMOS circuits

Christian Enz, Professor (Emeritus) École Polytechnique Fédérale de Lausanne

10:00 – 10:30 : POSTER SESSION-I

Entrance Hall, Chair: Lotte Geck

P.1 Prediction of Single Event Transient Propagation Using Machine Learning Models
Marko Andjelkovic, Junchao Chen, Jelisaveta Aleksic, Vishnu Padmakumar, Milos Marjanovic, Nikolaos Zazatis, Trupti Ranjan Lenka, Danijel Dankovic, Christos Sotiriou and Fabian Vargas

P.2 Design of a Low-Noise Amplifier for Qubit Readout
Gabriel López-Pinar, Uxua Esteban-Eraso, Santiago Celma and Carlos Sánchez-Azqueta

P.3 Ternary PUF-based Secure Mutual Authentication Using RNNs for Sequence Learning in Response Classification
Joseph He Chang, Shekoufeh Neisarian, Nico Mexis, Nikolaos Athanasios Anagnostopoulos, Tolga Arul and Elif Bilge Kavun

P.4 An Efficient Framework for Fully Automated Post-layout Simulation-based Optimization
Veeti Lahtinen, Altti Heikkinen, Santeri Porrasmaa, Aleksi Tamminen and Marko Kosunen

P.5 Designing compact phase shifters with a resistorless quadrature signal generator
Uxua Esteban Eraso, Carlos Sánchez-Azqueta, Francisco Aznar, Concepción Aldea and Santiago Celma

P.6 Fast and Accurate Multi-Neural Network Ensemble Model
Veli Nakçi and Mustafa Altun

10:30 – 11:00 : COFFEE BREAK

11:00 – 12:40 : SESSION-IV

Regular Session-5: Machine Learning and Simulation Methods for Advanced EDA

Room: Ömer Cerid, Chair: Jose De La Rosa

11:00 - 11:20: An AI-driven EDA Algorithm-Empowered VCO and LDO Co-Design Method
Yijia Hao, Maarten Strackx, Miguel Gandara, Sandy Cochran and Bo Liu

11:20 - 11:40: An Open-Source EM Simulation Flow Based on a High-Level Python API
Çağlar Özdağ, Engin Afacan and Gunhan Dundar

11:40 - 12:00: EMSpice 2.1: A Coupled EM and IR Drop Analysis Tool with Joule Heating and Thermal Map Integration for VLSI Reliability
Subed Lamichhane, Haotian Lu and Sheldon X.-D. Tan

12:00 - 12:20: On the Exploration of Convolutional Variational Autoencoders for Analog Integrated Circuit Post-Placement Performance Regression
Carlos Almeida, Marco Oliveira and Ricardo Martins

12:20 - 12:40: Design Space Exploration and Topology Assessment of Low-Power Sleep Comparators Using Evolutionary Algorithms
Enes Sağlıcan, Hakan Taşkıran, Kemal Ozanoglu and Engin Afacan

Regular Session-4: Circuit and System Design for Modern Communications

Room: Haliç, Chair: Mustafa Berke Yelten

11:00 - 11:20: A 1 Gb/s PAM-8 Variable-Gain Transimpedance Amplifier (VG-TIA) in 180 nm CMOS Technology
Fikriye Elif Karakuzu, Eray Kutuk, Arda Yıldız, İrem Cömertoğlu, Ali Doğuş Güngördu and Mustafa Berke Yelten

11:20 - 11:40: SystemVerilog-Based Modeling and Verification of 40-Gb/s/Lane PAM-3 Transmitter for USB4.0 Gen4
Yong-Gyu Yu, Ju-Hyeong Yun, Chae-Hyeon Lim and Joo-Hyung Chae

11:40 - 12:00: Dynamic Analysis of OOK Modulators Using Eye Diagrams to Assess Data Rate and Output Matching
Ahmet Yelboğa and Korkut K. Tokgöz

12:00 - 12:20: SystemVerilog-Based Modeling and Verification of 25.6-GBaud/Lane PAM-3 Receiver
Chae-Hyeon Lim, Ju-Hyeong Yun, Yong-Gyu Yu and Joo-Hyung Chae

12:20 - 12:40: Agile Frequency Synthesis for a sub-100uW Wake-up Receiver
Shaheeda Vajrala and Javed G S

12:40 – 14:00 : LUNCH BREAK

14:00 – 15:30 : SESSION-V

EDA Competition Session-2

Room: Ömer Cerid, Chair: Revna Acar Vural and Baykal Sarıoğlu

14:00 - 14:30: Technology-independent Layout Generator of Industry-grade Power Devices Validated Down to 22-nm Nodes
Duarte Marques, Ricardo Martins and Marcelino Santos

14:30 - 15:00: RadiSPICE-L: A Layout-Centric Tool for Radiation-Aware Analog Circuit Design
Ömer Yusuf Muhikanci, Kemal Ozanoglu, Günhan Dündar and Engin Afacan

15:00 - 15:30: ATOMIC: Automatic Tool for Memristive IMPLY based Circuit-level Simulation and Validation
Fabian Seiler, Peter M. Hinkel, Axel Jantsch and Nima Taherinejad

Special Session-2: Alternative Emerging Microsystems: MEMS, Microfluidics, and Photonic ICs

Room: Haliç, Chair: Onur Ferhanoğlu and Dağhan Gökdel

14:00 - 14:20: A Microfluidic Refreshable Braille Display System
Ömer Gökalp Akcan, Özlem Koçoğlu, Ahmet Can Erten and Onur Ferhanoğlu

14:20 - 14:40: Anisotropic and Tunable Vocal Fold Phantom for Biomechanical Modeling
Afarin Sarrafzadeh, Kuter Erdil, Onur Ferhanoglu and Ahmet Can Erten

14:40 - 15:00: Response Time Analysis of Thin Film Based Piezoresistive Pressure Sensor
Mehmet Akif Ozkaya, Kaan Demirel, Tugberk Taha Yolcu and Korkut Kaan Tokgoz

15:00 - 15:20: Thermal Modeling of Silicon Photonic Waveguides
Matthias Thiele, Jens Lienig, Menglong He and Kambiz Jamshidi

15:30 – 16:00 : COFFEE BREAK

16:00 – 17:20 : SESSION-VI

Regular Session-6: Modern IC Sizing and Layout Methods

Room: Ömer Cerid, Chair: Jürgen Scheible

16:00 - 16:20: Inverse Analog IC Sizing and Exploration through Diffusion Models and Structural Knowledge
Filipe Azevedo, Markus Leibl, Ricardo Martins and Helmut Graeb

16:20 - 16:40: Process-Portable Layout Generation of High-Speed Digital Circuit Using Standard Cells in FinFET
Taeseung Kang, Taeho Shin, Heejun Kim and Jaeduk Han

16:40 - 17:00: Technology-Independent Local Mismatch Estimation Using Precomputed Lookup Tables
Kareem Khattab, Muh-Dey Wei and Renato Negra

17:00 - 17:20: *Efficient Guard Ring-Aware Placement for FinFET Analog Circuits with Diffusion Sharing*
Shih-Yu Chen, Tzu-Hsiang Wei, Haoju Chang, Hung-Ming Chen and Chien-Nan Jimmy Liu

Special Session-3: Next-Generation Design Methodologies for High-Efficiency Sensor Systems

Room: Haliç, Chair: Ralf Sommer

16:00 - 16:20: Application of the Expert Design Plan Methodology on an Ultra-Low-Power Sensor Frontend
Lorenz Renner, Ralf Sommer and Yannick Uhlmann

16:20 - 16:40: Temperature Sensors in FPGA Based On Digital Nonlinear Oscillators for Improved Sensitivity
Raúl Aparicio-Téllez, Miguel Garcia-Bosque, Guillermo Diez-Señorans and Santiago Celma

16:40 - 17:00: A Low-Voltage, Low-Power CMOS Temperature Sensor Utilizing a Single PTAT-CTAT Current Loop
Tugce Karpuz, Kemal Ozanoglu and Sumer Can

17:00 - 17:20: A QCM-VNA System for Microfluidic Sensing: Leveraging Higher-Order Harmonics
Eren Koltuk, Saibe Demir, Eren Yalçın, Kerim Alaz Demir, Ebrar Kahveci, Okan Zafer Batur, Günhan Dündar and Ceyhun Ekrem Kırımlı

19:00 – 22:00 GALA DINNER

DAY-4

Thursday

10.07.2025 | 08:00 - 17:30

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09:00 – 10:00 : KEYNOTE TALK

Room: Ömer Cerid
Chair: Günhan Dündar

Supply chain vulnerabilities for ICs and Mitigation Through Design-for-Trust

Ozgur Sinanoglu, Professor, Electrical and Computer Engineering, New York University Abu Dhabi, UAE

10:00 – 10:30 : POSTER SESSION-II

Entrance Hall, Chair: Lida Kouhalvandi

P.6 Simulink-Based HDL Design: A Case Study on Harmonic Control Arrays Algorithm Realization
Akif Altintas, Muhammed Yusufoglu, Ugur Cini and Murat Dogruel

P.7 Trust Based Access Control For Dynamically Reconfigurable Sensor Network
Mehmet Onur Demirturk and Berna Ors

P.8 WDP: A Weighted Delay Prediction Method for Integrated Circuit Interconnects
Yoonsoo Park, Songnam Hong and Jaeduk Han

P.10 Optically Powered Sub-1 dB Noise Figure CMOS LNA for Magnetic Resonance Imaging
Mert Şentürk, Günhan Dündar and Arda Deniz Yalçınkaya

P.11Power Amplifier Modeling along with Hyperparameter Optimization of LSTM-based DNN through Multi-Verse Optimizer
Lida Kouhalvandi, Sercan Aygun, Serdar Ozoguz, Ladislau Matekovits, M. Hassan Najafi and Saeid Karamzadeh

P.12 Simulation Study of the Maximum Power Dissipation-Energy Consumption Dilemma in Memristors Using the Dynamic Memdiode Model
Enrique Miranda, Eszter Piros, Fernando Aguirre, Xavier Pérez, Taewook Kim, Philipp Schreyer, Jonas Gehrunger, Timo Oster, Klaus Hofmann, Jordi Suñé, Chirstian Hochberger and Lambert Alff

10:00 - 11:00 TICA presentation

Room: Ömer Cerid

Presenter: *Prof. Yusuf Leblebici*

Turkish Integrated Circuits Alliance (TICA) will be introduced by the president of TICA.

10:30 – 11:00 : COFFEE BREAK

11:00 – 12:40 : SESSION-VII

Regular Session-7: Reinforcement Learning for Analog/RF Circuit Design Communications

Room: Ömer Cerid, Chair: Engin Afacan and Ricardo Martins

11:00 - 11:20: Enhancing Reinforcement Learning for the Floorplanning of Analog ICs with Beam Search
Sandro Junior Della Rovere, Davide Basso, Luca Bortolussi, Husni Habal and Mirjana Videnovic-Misic

11:20 - 11:40: On the Usage of Genetic Algorithms, Reinforcement Learning and Bayesian Optimisation for RF IC Design Automation
Margarida Baptista Lourenço, Zhao Bingbing, Li Junde, Marcelino Santos, Pui-In Mak, Rui Martins, Wei-Han Yu and Fábio Passos

11:40 - 12:00: Multi-Objective Optimization of Analog Circuits Using Reinforcement Learning
Hakan Taşkıran, Enes Sağlıcan and Engin Afacan

12:00 - 12:20: A Comparative Study on the Incorporation of PVT Corner Conditions within Reinforcement Learning-based Analog IC Sizing Approaches
José Costa, Filipe Azevedo and Ricardo Martins

12:20 - 12:40: An Open-Source Environment for Evaluating Reinforcement Learning Algorithms for Analog IC Floorplanning
Till Moldenhauer, Yannick Uhlmann and Jürgen Scheible

Special Session-4: Advances in Neuromorphic Systems: Circuit Development and Applications

Room: Haliç, Chair: Tuba Ayhan

11:00 - 11:20: NNHC - a Neural Network to Hardware Compiler
Sascha Schmalhofer, Yasmine Abu-Haeyeh and Lars Hedrich

11:20 - 11:40: Ultra-Low Power and Low-Leakage Subthreshold CMOS Neural Circuit Design
Muhammed Efdal Elkatmış, Okan Zafer Batur and Burcu Erkmen

11:40 - 12:00: Modeling and Analysis of MS Accelerators Embedding SRAM and RRAM Compute Cells
Michele Caselli and Andrea Boni

12:00 - 12:20: Behavioral Modeling of Analog Neural Networks Inference Circuits
Yasmine Abu-Haeyeh, Sascha Schmalhofer and Lars Hedrich

12:20 - 12:40: A Practical PCB-based Framework for Spiking Neural Networks with a Half-Adder Example
Sevde Vuslat Çıkıkçı, Eren Örek, Ayhan Aysoy, Ali Kağan Özgen, Arda Yavuz and Tuba Ayhan

12:40 – 14:00 : LUNCH BREAK

14:00 – 15:20 : SESSION-VIII

Regular Session-8: Energy Efficiency Frontiers: SRAM, DLDOs, and Neural Stimulators

Room: Ömer Cerid, Chair: Lobna Said

14:00 - 14:20: 1/2 Ccell Vdd^2? An Energy Model for Compute-in-Memory SRAM Cells
Simon Wilhelmstätter, Joschua Conrad, Johannes Stark, Devanshi Upadhyaya, Maël Gay, Ilia Polian and Maurits Ortmanns

14:20 - 14:40: A Comparative Study of Switch-Mode and Constant-Current Methods for High-Efficiency Neural Stimulation
Sergio Massaioli and Georges Gielen

14:40 - 15:00: A Hysteretic-Controlled Digital LDO Regulator for Enhanced Load Transient Response
Kartikay Tripathi, Madhav Pathak, Sanjeev Manhas and Anand Bulusu

15:00 - 15:20: SPFD-Based Delay Resynthesis
Andrea Costamagna, Chang Meng and Giovanni De Micheli

Regular Session-9: Advances in Hardware Security

Room: Haliç, Chair: Elif Bilge Kavun

14:00 - 14:20: Towards a Reliable PUF Using Organic Thin-Film Transistors
Fernando de Los Santos Prieto, Deborah Eric, Marc Porti, Rafael Castro López, Elisenda Roca, Francisco V. Fernández and Montserrat Nafria

14:20 - 14:40: Multimodal IoT Device Authentication using Behavioral and Physical Unclonable Functions and Kyber Public Key Encryption
Roberto Román, Rosario Arjona and Iluminada Baturone

14:40 - 15:00: TERORO - Transient Effect Ring Oscillator and Ring Oscillator Configurable Hybrid PUF
Alejandro Casado-Galán, Juan Núñez-Martínez, Erica Tena-Sánchez, F. Eugenio Potestad- Ordóñez and Antonio Acosta

15:00 - 15:20: Fault Injection Attacks Based on Layout-Driven SER Analysis
Alexandra Takou, Pelopidas Tsoumanis, Georgios-Ioannis Paliaroutis, Nestor Evmorfopoulos and George Stamoulis

15:20 – 15:50 : COFFEE BREAK

15:50 – 16:50 : SESSION-IX

Regular Session-10: Novel Techniques for Reliability and Fault Detection/Prediction

Room: Ömer Cerid, Chair: Günhan Dündar

15:50 - 16:10: Hybrid AI-Optimization Method for Latent Defect Detection Through Test Insertion in Analog circuits
Sankhya Bhattacharya and Georges Gielen

16:10 - 16:30: A Power-Efficient Analog Integrated Decision Tree Classifier for Machine Predictive Maintenance Classification
Vassilis Alimisis, Konstantinos Cheliotis, Vasileios Moustakas, Anna Mylona, Zisis Foufas and Paul P. Sotiriadis

16:30 - 16:50: Compact SER Models via Model Order Reduction of Diffusion-Based Charge Collection
Pavlos Stoikos, Olympia Axelou, Pelopidas Tsoumanis, Georgios-Ioannis Paliaroutis and George Floros

Regular Session-11: Device and Circuit Modeling

Room: Haliç, Chair: Francisco V. Fernandez

15:50 - 16:10: 3D Monte Carlo Simulations of n-type Nanowire-FETs: The Effect of Gate Scaling
Murad Alabdullah, Natalia Seoane, Antonio García Loureiro and Karol Kalna

16:10 - 16:30: Dark Current Analysis in Silicon PIN Photodetectors: TCAD, Lifetime and Statistical Process Control
Yigithan Mehmet Kose, Utku Guney, Elcin Mert and Dilek Alimli

16:30 - 16:50: Integration of CMOS Photodiode and Capacitive Charge Pump Circuits for On Chip Photovoltaic Energy Harvesting
Macit Uluda, Ali E. Oktem, Gunhan Dundar and Arda D. Yalcinkaya

17:00 – 18:00 Closing Remarks and Awards Ceremony