EPFL

The sEKV Model for the Design of Cryo-CMOS Circuits

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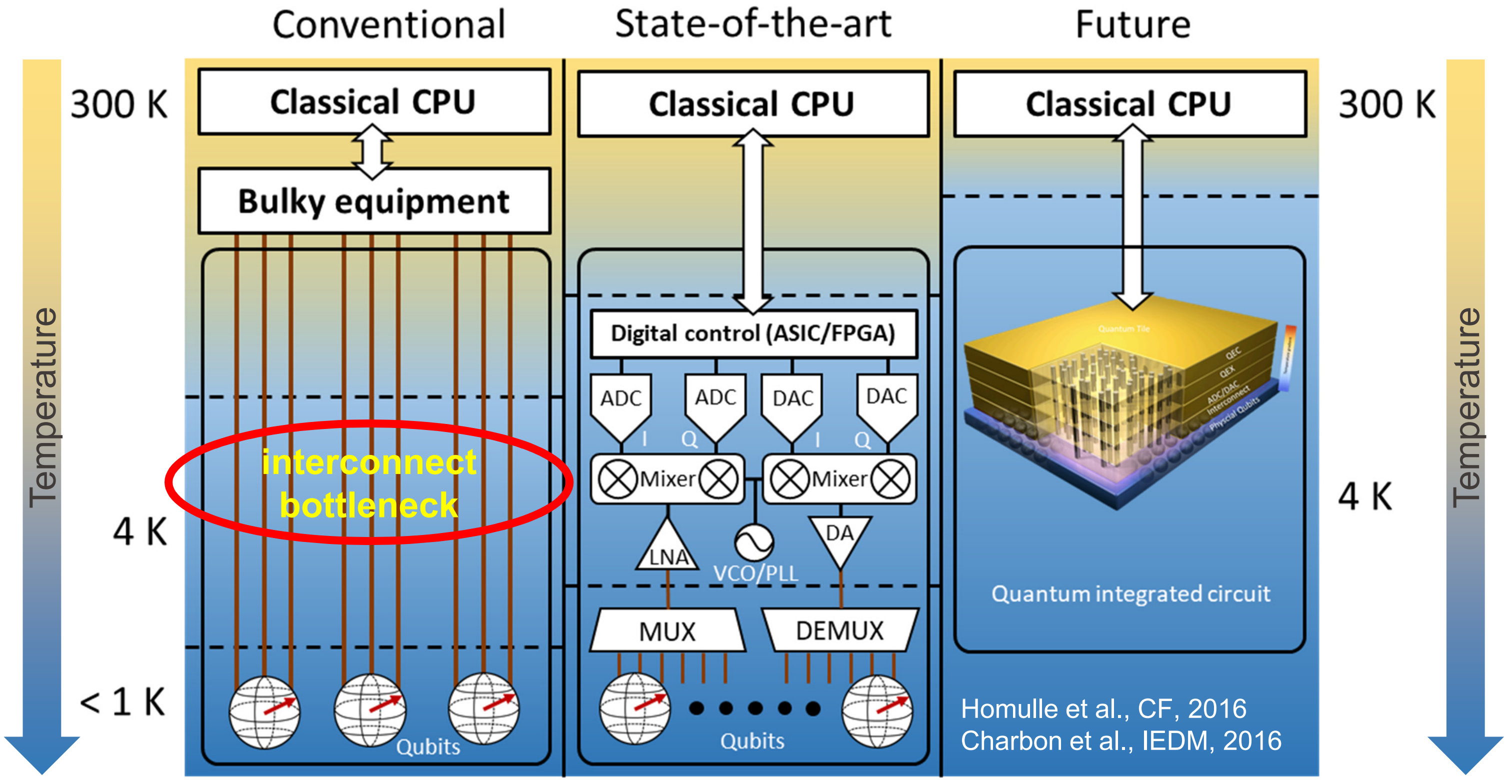
Outline

- Introduction
- Subthreshold current and swing
- Threshold voltage
- Simplified EKV model at CT
- RF modeling
- Noise modeling
- Conclusion

The Quest for the Quantum Integrated Circuit



H. Homulle, *et al.*, ACM International Conference on Computing Frontiers, May 16, 2016.
E. Charbon, *et al.* IEDM 2016.

Reduction of T down to Cryogenic Temperature (CT)

Parameter	CT Behavior	Impact
Mobility	Increases	☺
Saturated velocity	Increases	☺
Transconductance	Increases	☺
Subthreshold swing (SS)	Decreases, but saturates at LT	☺ ☹
Leakage currents	Decrease	☺
Thermal conductivity	Increases	☺
Thermal noise	Decreases	☺
Flicker noise	Increases	☹
Threshold voltage	Increases	☹
Oscillations and kinks in the transfer and output characteristic	Appear	☹

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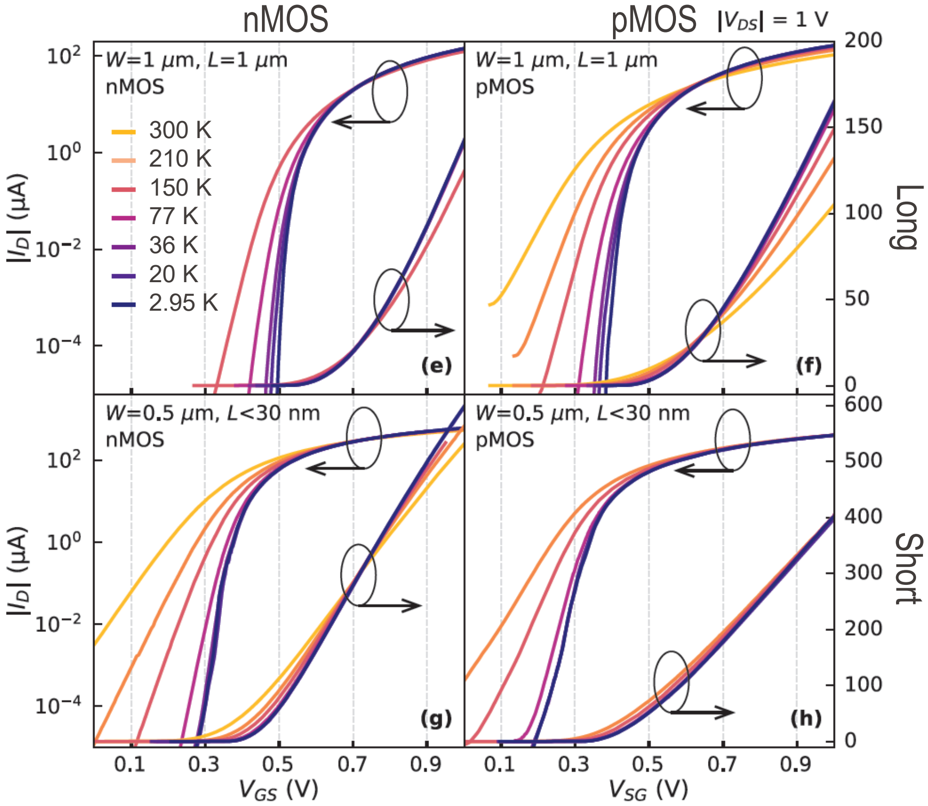
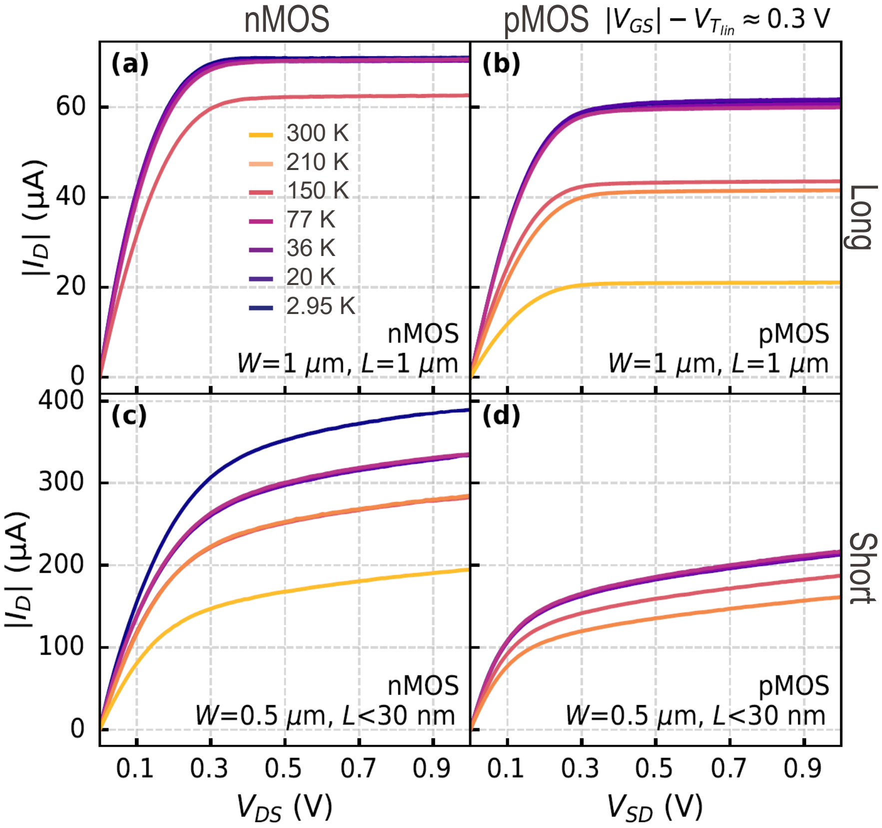
I-V Characteristics of 22 nm FDSOI

Transfer Characteristic in Saturation

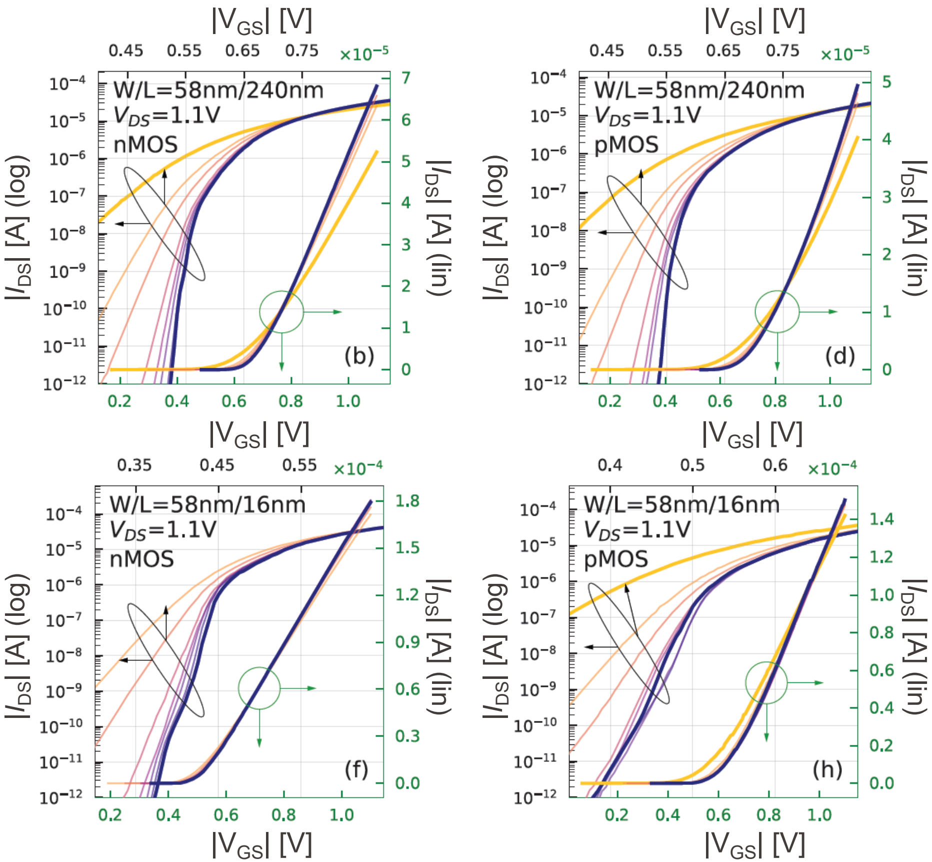


Output Characteristic in Strong Inversion

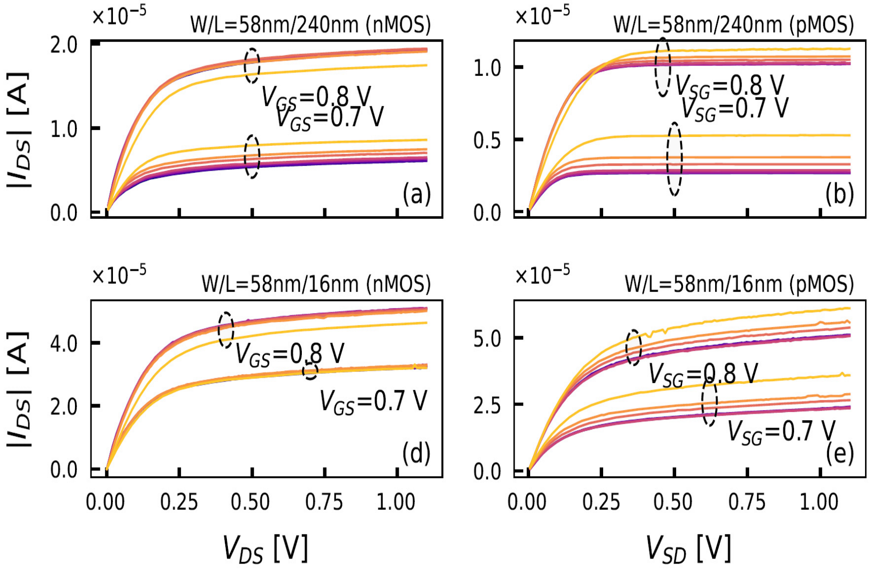


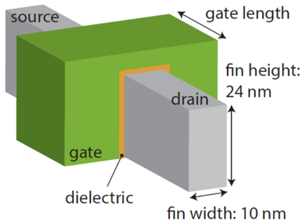
I-V Characteristics of 16nm FinFET

Transfer Characteristic in Saturation

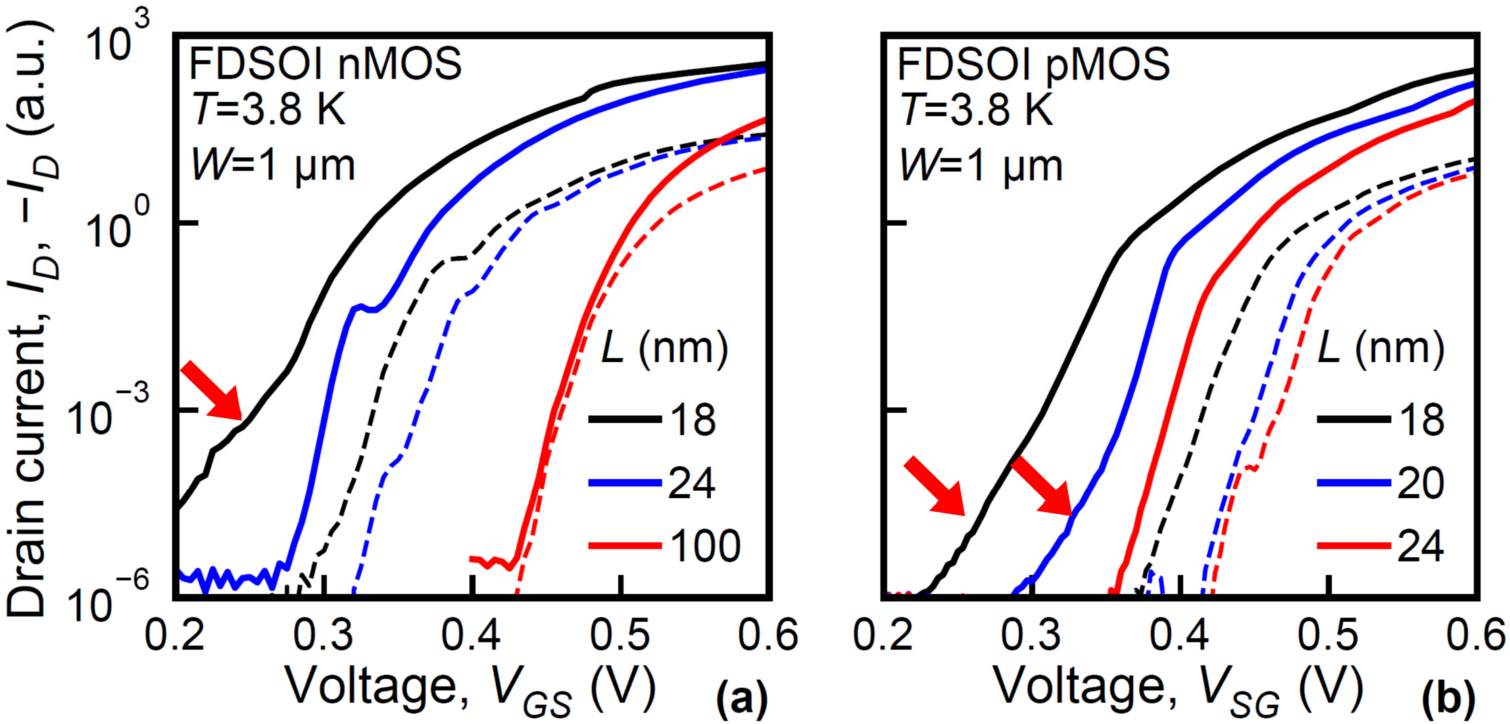


Output Characteristic in Strong Inversion



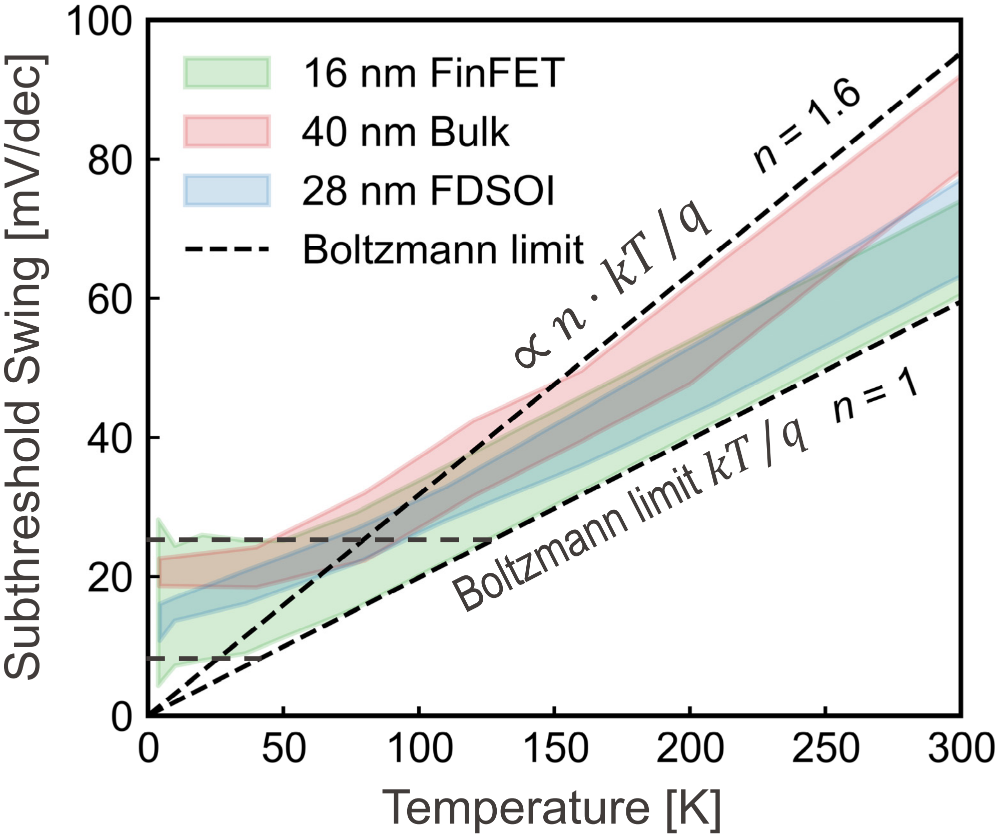


Subthreshold Current



Dashed lines: $V_{DS} = 10\ mV$ (linear)
Solid lines: $V_{DS} = 0.8\ V$ (saturation)

Subthreshold Swing SS



$$SS \triangleq \left(\frac{d\ \log_{10} I_D}{d\ V_G}\right)^{-1} = \frac{\partial V_G}{\partial \varphi_{ch}} \cdot \left(\frac{d\ \log_{10} I_D}{d\ \varphi_{ch}}\right)^{-1}$$

$$= n \cdot \ln 10\ \frac{kT}{q}$$

Electro static control

Thermionic current

Impact of SS Saturation on Power

- Required current to achieve a given **transconductance** G_m in weak inversion

$$I_D = G_m \cdot n_{eq} \cdot U_T$$

- with $U_T \triangleq \frac{kT}{q}$ and where n_{eq} is defined as

$$n_{eq}(T) = \frac{SS(T)}{\ln 10 \; U_T} = \begin{cases} n & \text{for } T_c < T \\ \frac{q}{\ln 10} \cdot \frac{SS_{sat}}{kT} & \text{for } T < T_c \end{cases}$$

- **Current savings** at CT to reach the same G_m than at RT in weak inversion

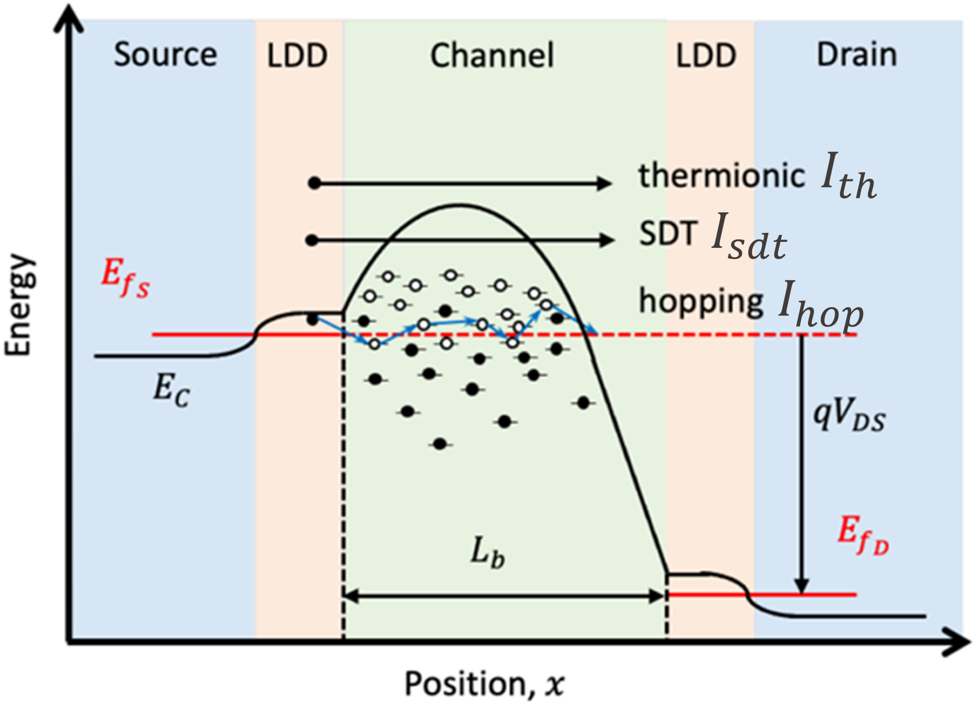
$$\frac{I_D|_{cryo}}{I_D|_{RT}} = \frac{n_{eq}|_{cryo}}{n_{eq}|_{RT}} \cdot \frac{T_{cryo}}{T_{RT}} = \frac{33}{1.5} \cdot \frac{4.2}{300} = 22 \cdot \frac{1}{71} = \frac{1}{3.2}$$

- Current savings of 3.2 instead of 70 if n_{eq} would remain constant

C. Enz, H.-C. Han, "Design of Cryo-CMOS Analog Circuits using the G_m/I_D Approach," ISCAS 2023.

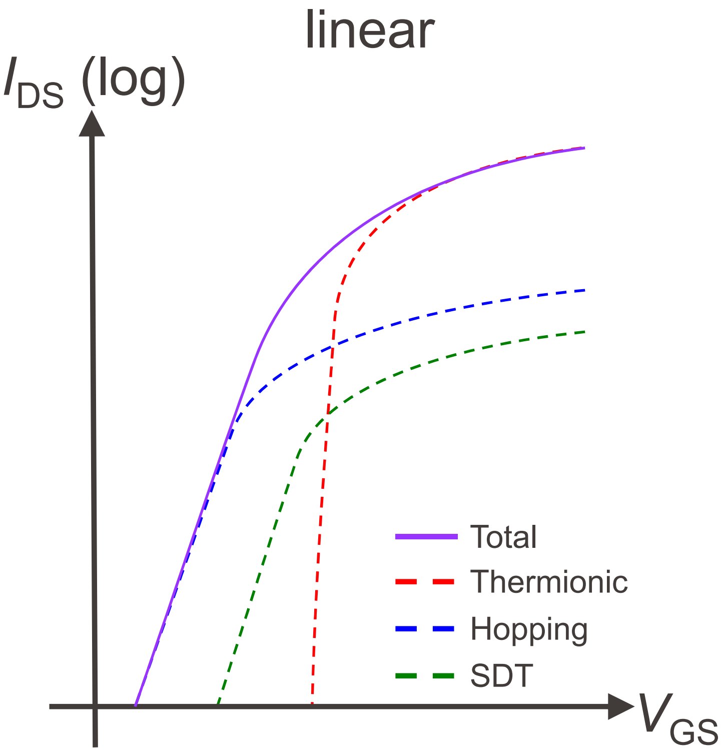
Subthreshold Drain Current

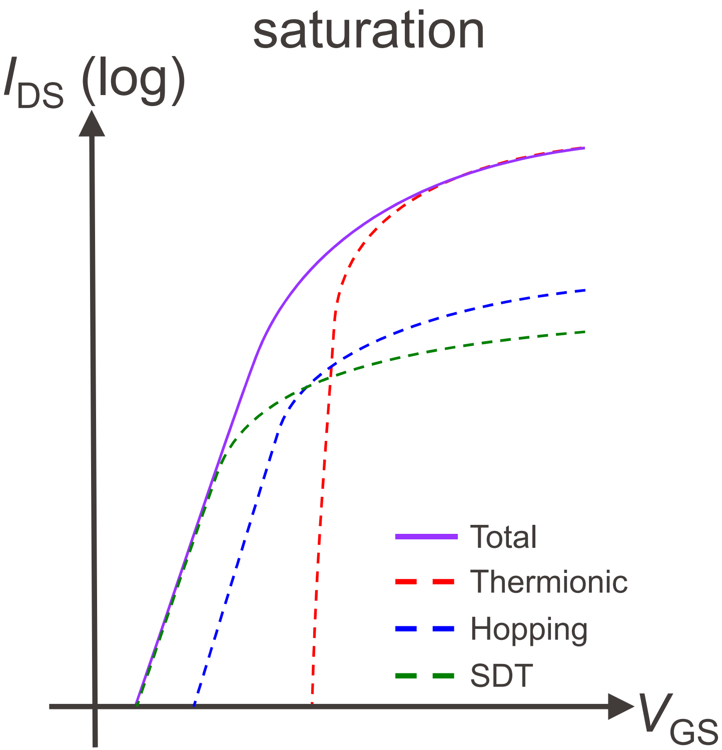
$$I_{sub} = I_{th} + I_{hop} + I_{sdt}$$



- The subthreshold drain current I_{sub} is made of
  $$I_{sub} = I_{th} + I_{hop} + I_{sdt}$$
- The **thermionic current** $\boldsymbol{I_{th}}$ which dominates at RT
- The **hopping current** $\boldsymbol{I_{hop}}$ in **band tail**
- The **source-to-drain tunneling current** $\boldsymbol{I_{sdt}}$

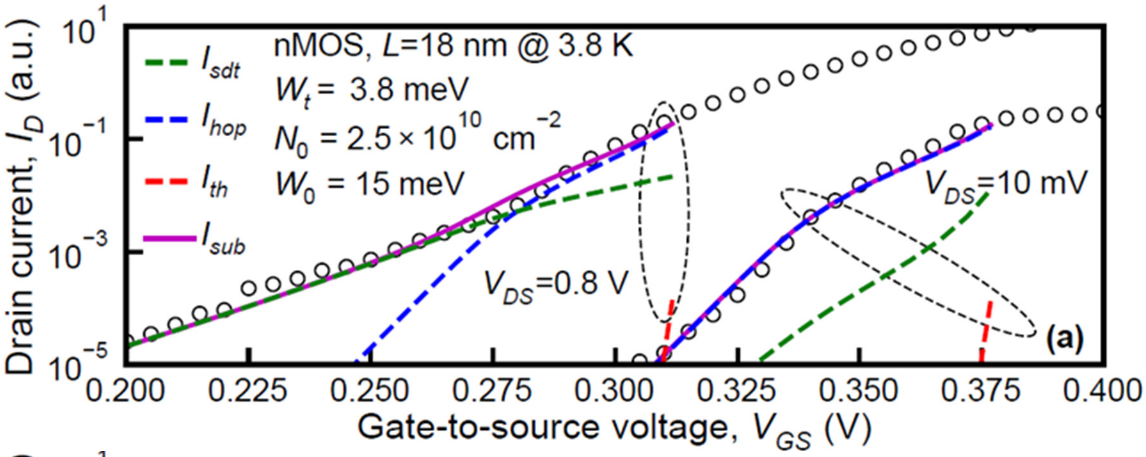
Subthreshold Currents at CT

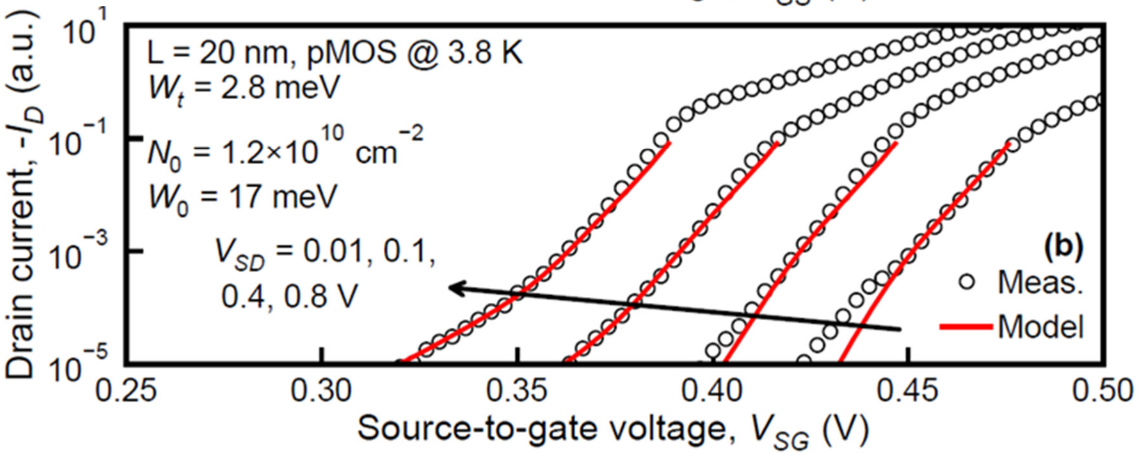




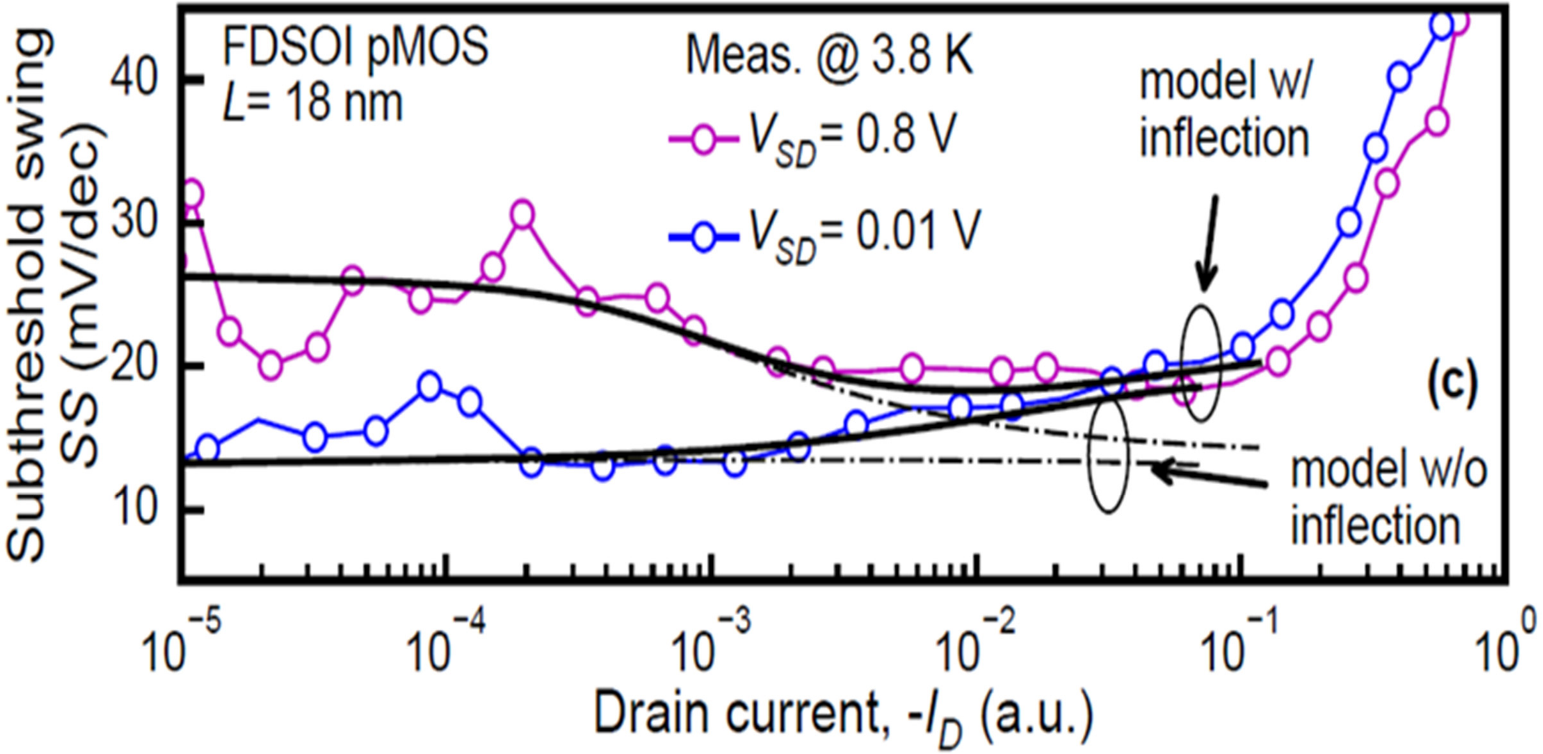
- Hopping current dominates
- SDT current dominates

Subthreshold Current Model Validation on 22nm FDSOI at CT



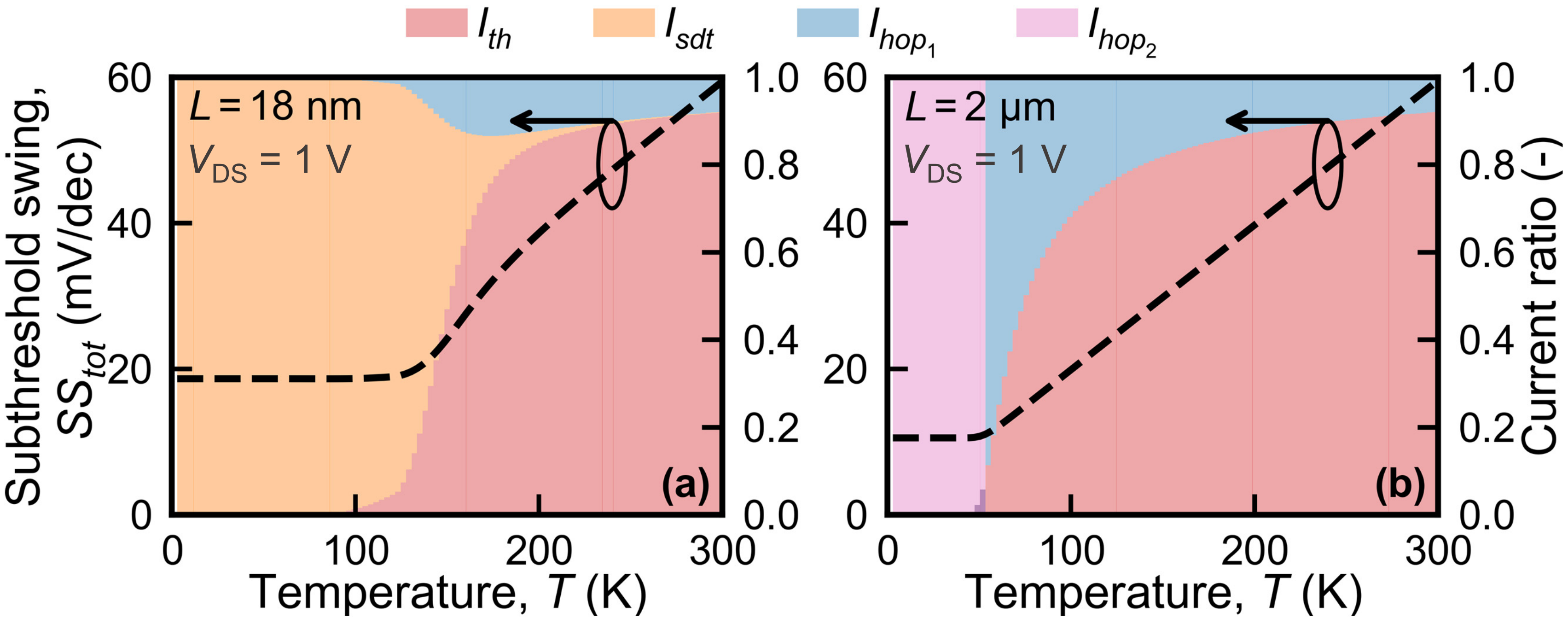


Subthreshold Swing Validation on 22nm FDSOI at CT



Current Decomposition and Subthreshold Swing

Short-channel in saturation | Long-channel in saturation



- Current dominated by SDT at CT
- Current dominated by hopping current I_{hop2} at CT

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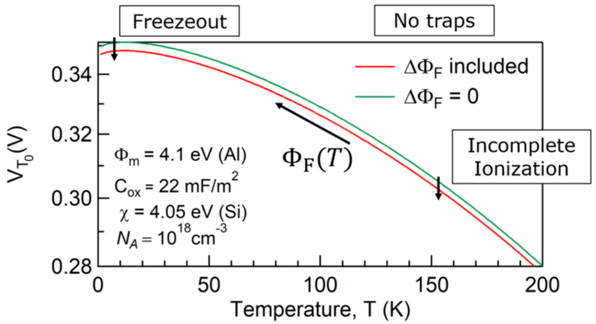
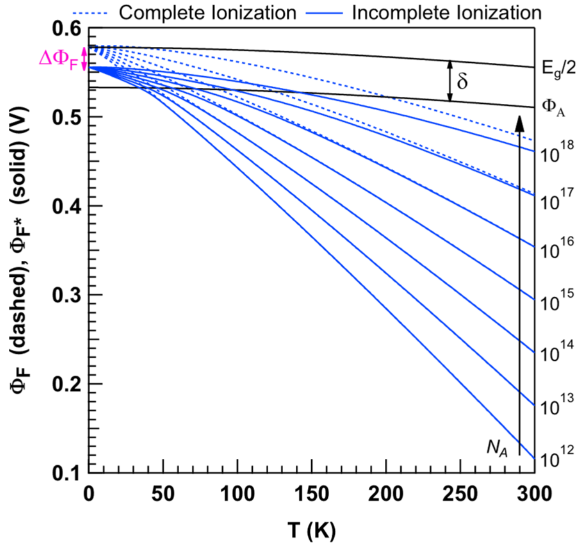
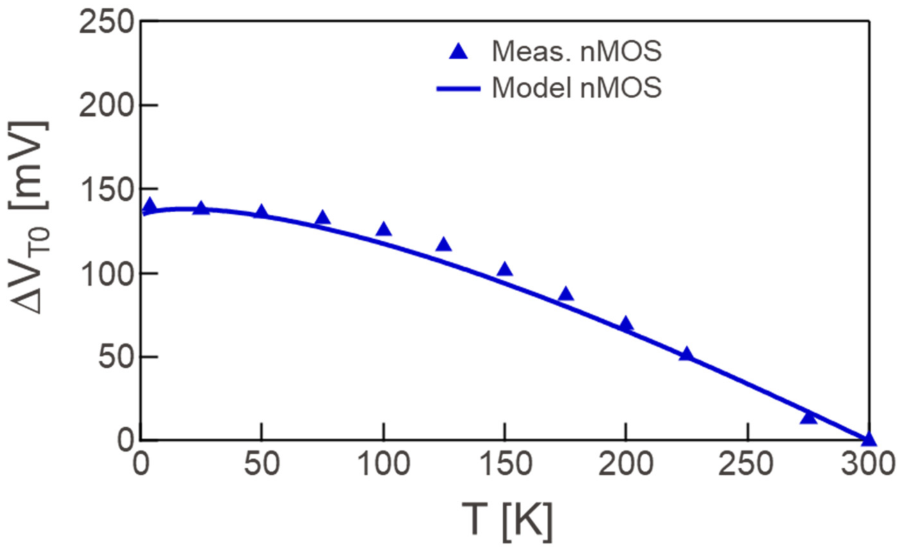
Threshold Voltage Modeling



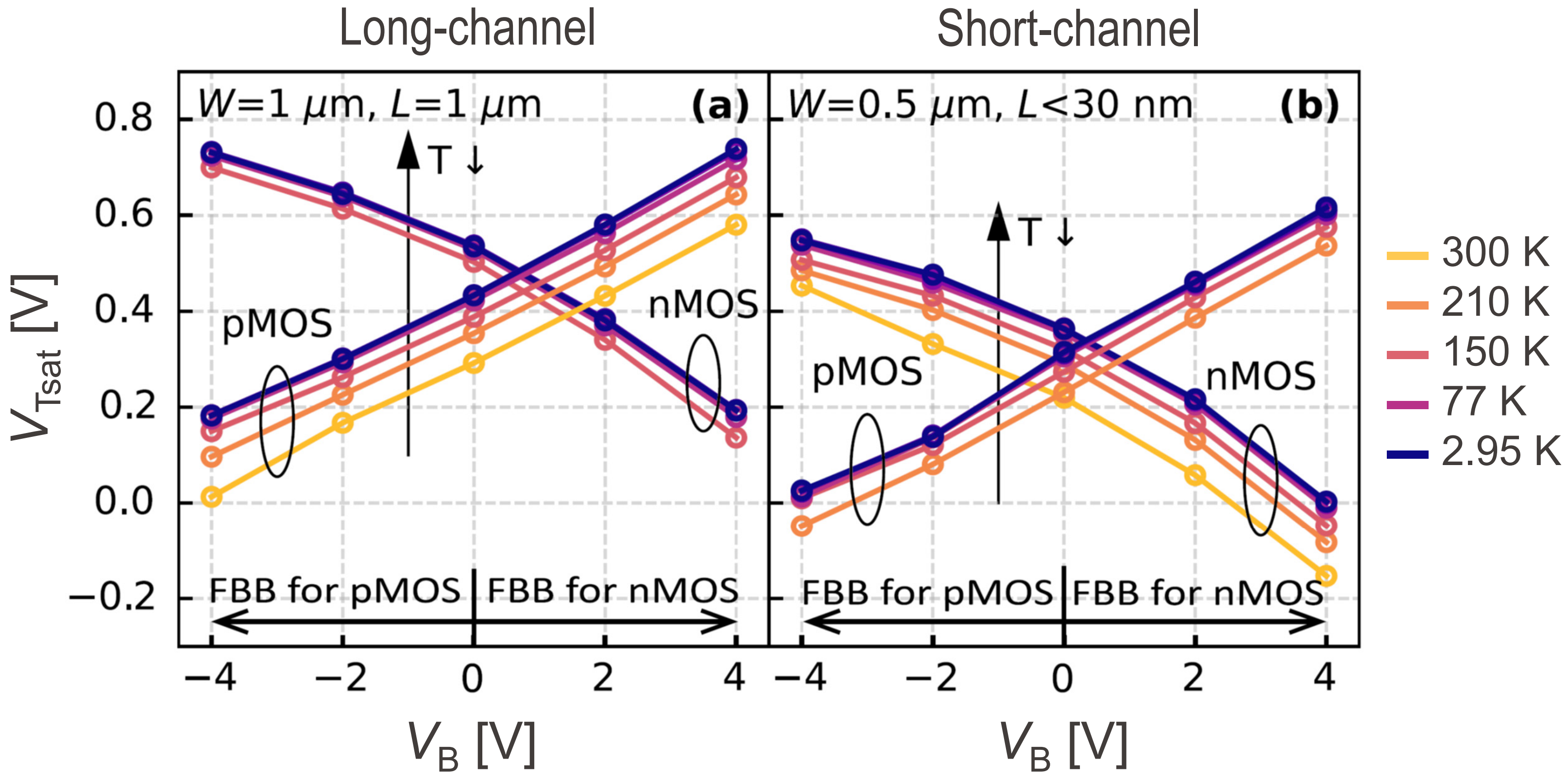




- ΔV_{T0} mostly due to change in the Fermi voltage as illustrated in the right figure
- Impact of incomplete ionization is minor

A. Beckers, *et al.*, IEEE JEDS, vol. 8, pp. 780–788, April 2020.

Threshold Voltage vs Back-gate Voltage



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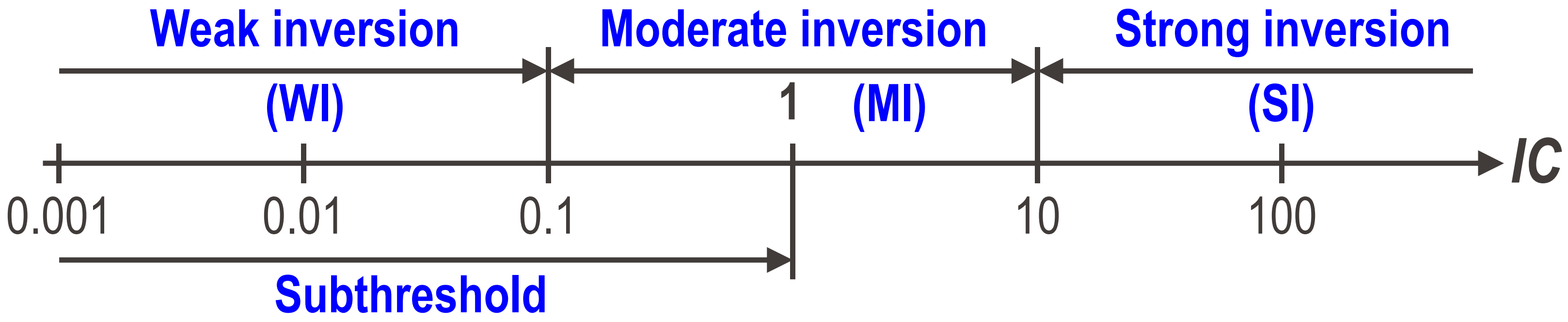
The Concept of Inversion Coefficient

- Overdrive voltage $V_G - V_{T0}$ not convenient for weak inversion
- Replaced by the **inversion coefficient IC** characterizing the global level of inversion of the transistor in **saturation**

$$IC \triangleq \frac{I_D|_{saturation}}{I_{spec}}$$

Typical values of $I_{spec\square}$ for 28-nm (at RT):
750 nA for NMOS
200 nA for PMOS

- where $I_{spec} = I_{spec\square} \cdot W/L$, $I_{spec\square} \triangleq 2n \cdot \mu \cdot C_{ox} \cdot U_T^2$, $U_T \triangleq kT/q$



C. Enz, F. Chicco, and A. Pezzotta, IEEE Solid-State Circuits Magazine, vol. 9, no. 3, pp. 26-35, Summer 2017.

Simplified EKV Charge-based Model (in saturation)

- The **normalized drain current** in saturation or **inversion coefficient** is given by

$$IC \triangleq \frac{I_D|_{saturation}}{I_{spec}} = \frac{4(q_s^2 + q_s)}{2 + \lambda_c + \sqrt{4(1+\lambda_c) + \lambda_c^2 \cdot (1 + 2q_s)^2}}$$

- where $q_s \triangleq Q_i(x=0)/Q_{spec}$ is the **normalized inversion charge** at the source with $Q_{spec} \triangleq -2n \cdot C_{ox} \cdot U_T$
- λ_c is the **velocity saturation** (VS) parameter corresponding to the fraction of the channel under full velocity saturation

$$\lambda_c \triangleq \frac{L_{sat}}{L}$$

- where $L_{sat} = 2\mu_0 \cdot U_T / v_{sat} = 2U_T/E_c$ is the channel length over which the velocity is fully saturated

C. Enz, F. Chicco, and A. Pezzotta, IEEE Solid-State Circuits Magazine, vol. 9, no. 3, pp. 26-35, Summer 2017.

Voltage versus Charge

- The current versus charge expression is coupled to the following **voltage versus charge** relation

$$v_p - v_s = ln(q_s) + 2q_s$$

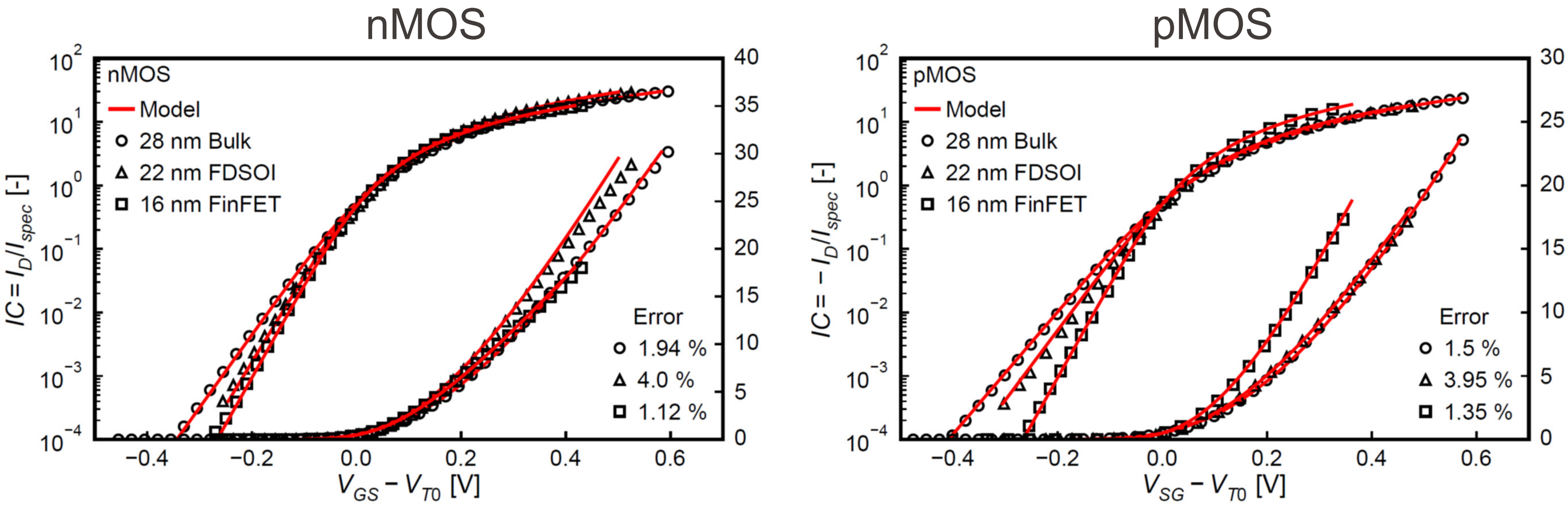
- where voltages are normalized to $U_T \triangleq kT/q$

$$v_p \triangleq \frac{V_P}{U_T} = \frac{V_G - V_T}{n \cdot U_T} \qquad v_s \triangleq \frac{V_S}{U_T} \qquad U_T \triangleq \frac{kT}{q}$$

- where $V_P = (V_G - V_T)/n$ is the **pinch-off voltage**
- Only requires the following **4 parameters:** V_T, $I_{spec\square}$, n, L_{sat} (or λ_c)
- No explicit expression of the current versus voltage
- Note that parameter n allows to change the slope factor versus temperature

C. Enz, F. Chicco, and A. Pezzotta, IEEE Solid-State Circuits Magazine, vol. 9, no. 3, pp. 26-35, Summer 2017.

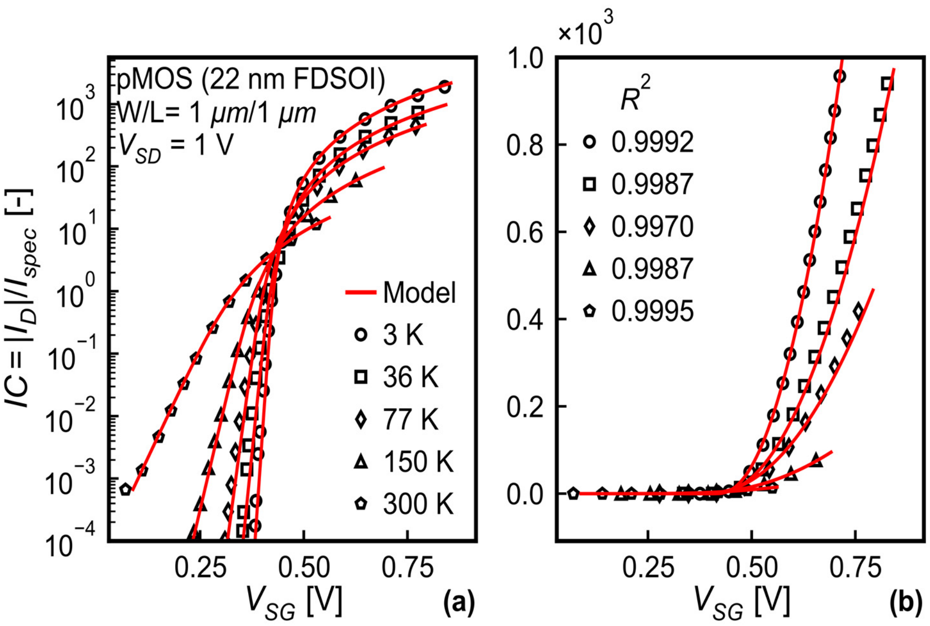
sEKV for Different Advanced Technologies (RT)

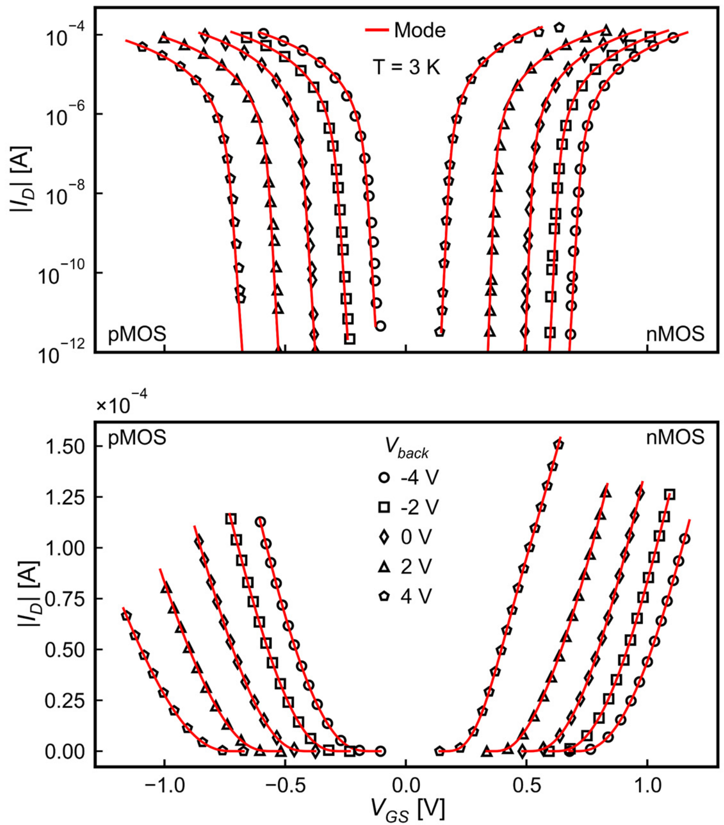


- The normalization process strips-off most of the technology dependence which is captured by only **4 parameters V_{T0}, $I_{spec\square}$, n, L_{sat}**

H. -C. Han, A. D'Amico and C. Enz, "SEKV-E: Parameter Extractor of Simplified EKV I-V Model for Low-Power Analog Circuits," OJCAS, vol. 3, pp. 162-167, 2022.

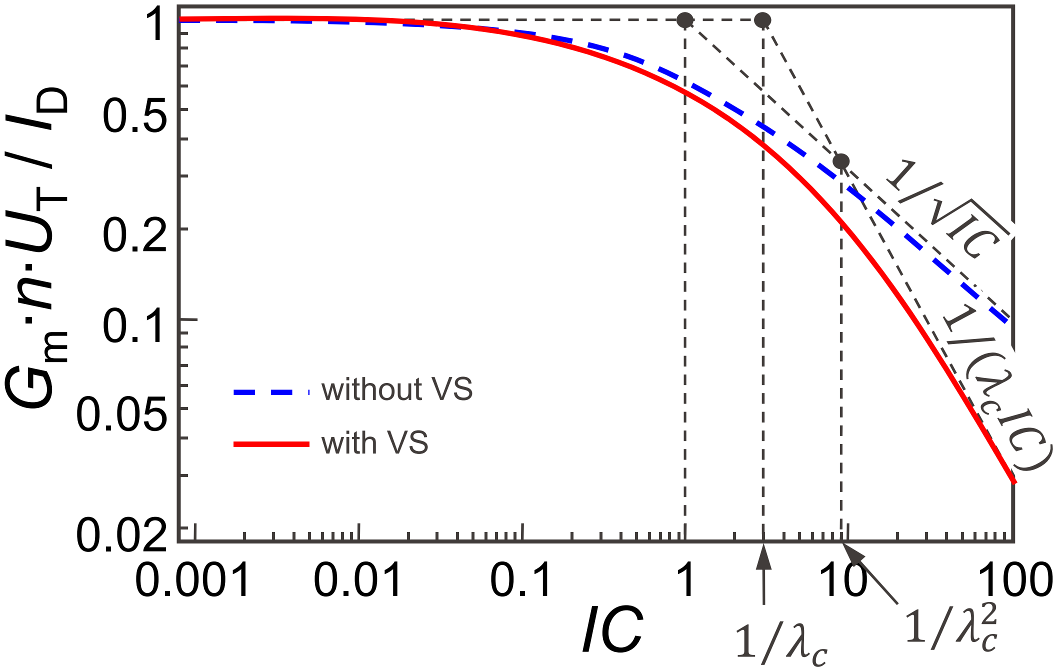
sEKV for 22nm FDSOI at Cryogenic Temperature





📖 H. -C. Han, A. D'Amico and C. Enz, "SEKV-E: Parameter Extractor of Simplified EKV I-V Model for Low-Power Analog Circuits," OJCAS, vol. 3, pp. 162-167, 2022.

Current Efficiency or G_m/I_D FoM



$$\frac{g_{ms}}{i_d} \triangleq \frac{G_{ms} \cdot U_T}{I_D} = \frac{G_m \cdot n \cdot U_T}{I_D}$$

$$= \frac{\sqrt{(\lambda_c IC + 1)^2 + 4IC} - 1}{IC \cdot [\lambda_c \cdot (\lambda_c IC + 1) + 2]}$$

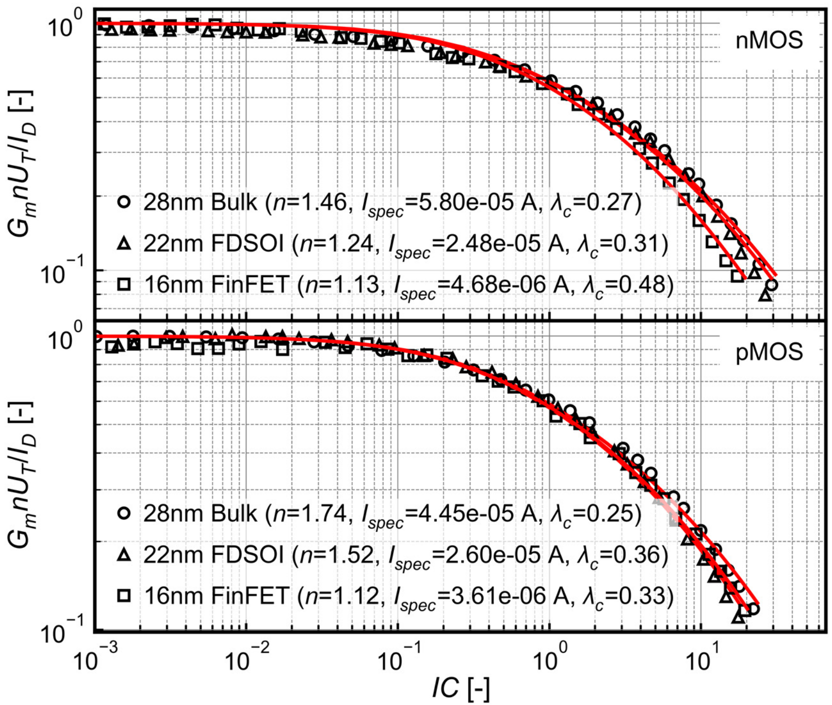
$$= \begin{cases} 1 & \text{WI and sat.} \\ \dfrac{1}{\lambda_c \cdot IC} & \text{SI and sat.} \end{cases}$$

$$\lambda_c \triangleq \frac{L_{sat}}{L}$$

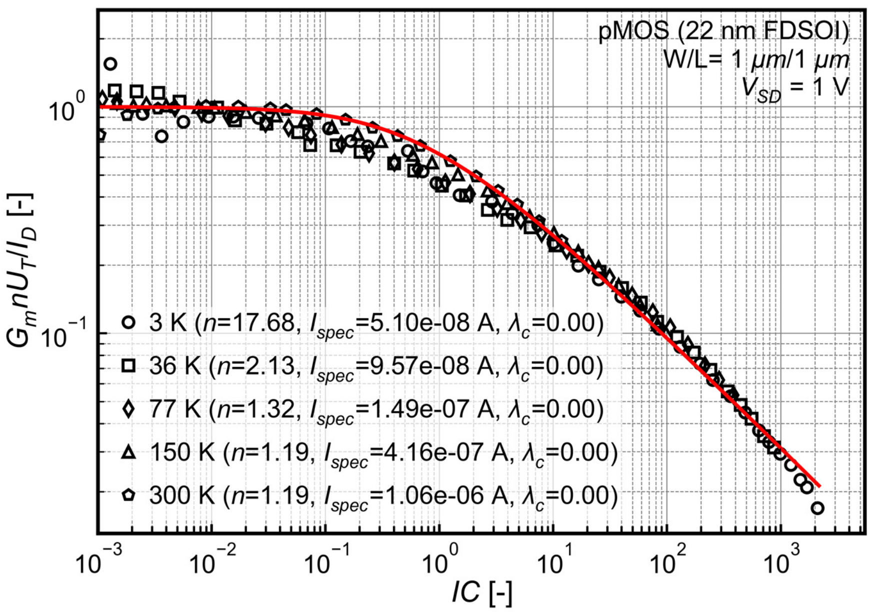
- The G_m/I_D FoM tells how much G_m you get for a given current
- It is a fundamental FoM for low-power analog and RF IC design

The G_m/I_D for Different Advanced Technologies

RT



RT down to CT



The normalized G_m/I_D FoM is **invariant to technologies**

The normalized G_m/I_D FoM is almost **independent of temperature**

H. -C. Han, A. D'Amico and C. Enz, "SEKV-E: Parameter Extractor of Simplified EKV I-V Model for Low-Power Analog Circuits," OJCAS, vol. 3, pp. 162-167, 2022.

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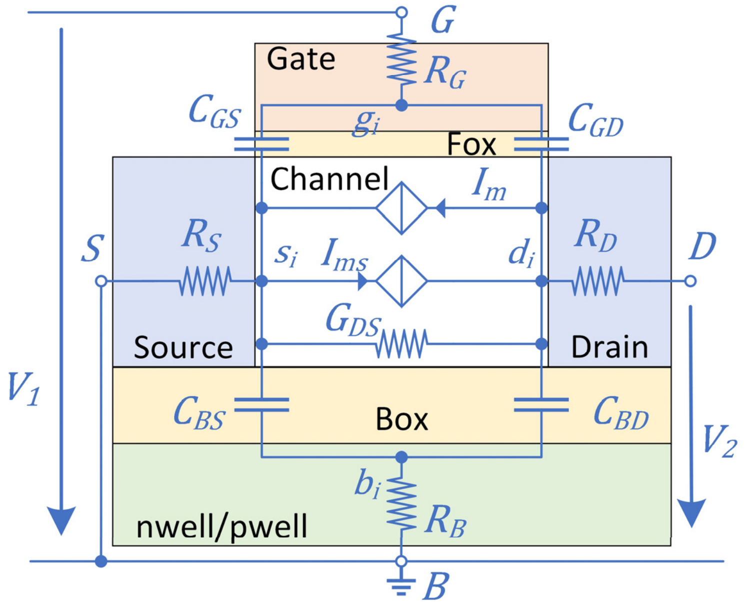
Simple RF modeling of FDSOI

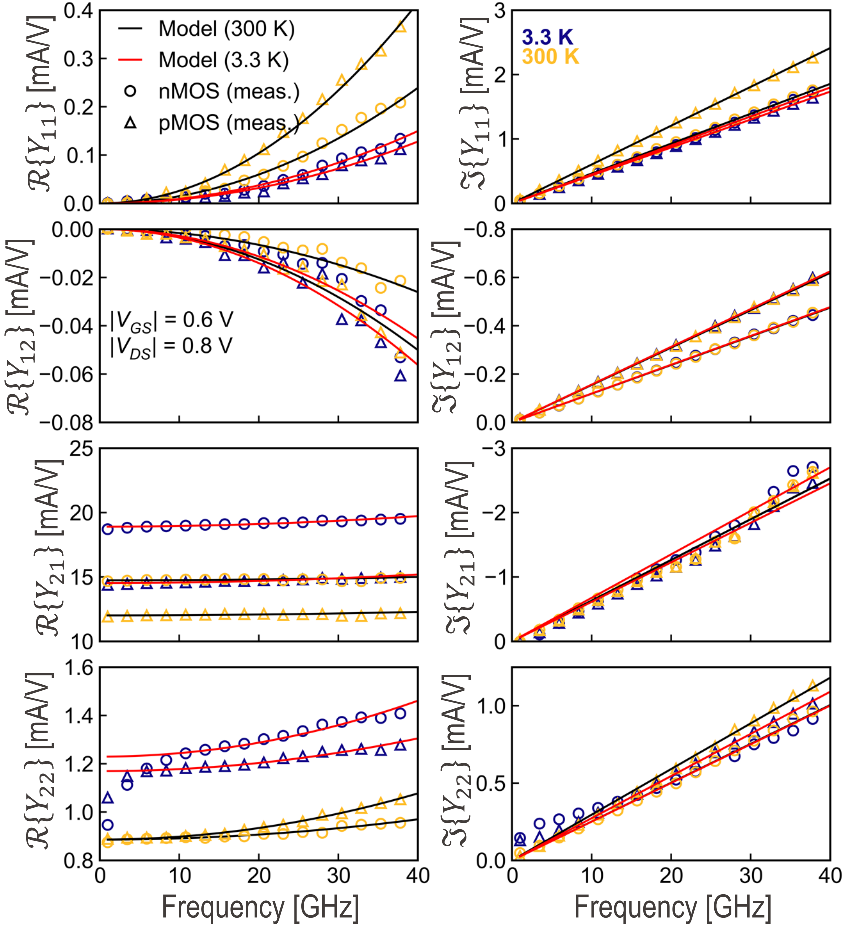


- Approximation of the Y−parameters given below
- $\Re(Y)$ shows quadratic behavior with respect to frequency
- It allows direct analytical parameter extraction (without optimization)

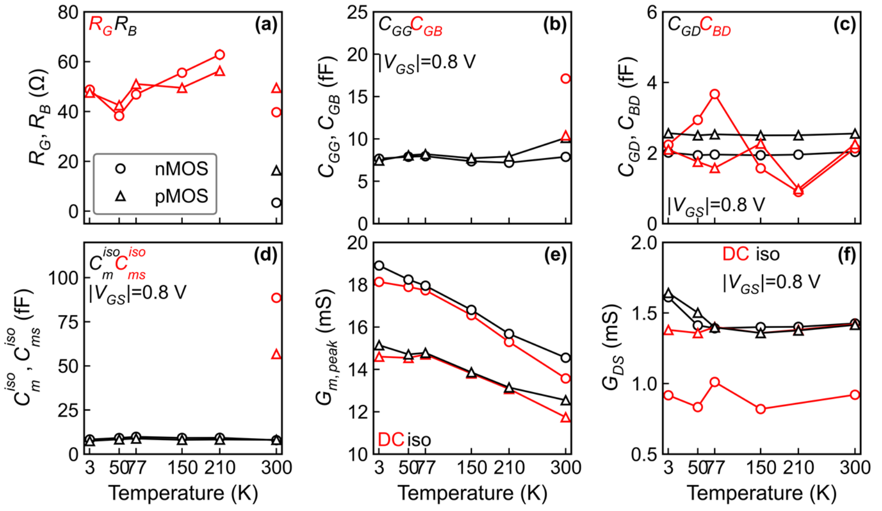
$$Y_{11} \cong \omega^2(C_{GB}^2 R_B + C_{GG}^2 R_G) - j\omega C_{GG}$$
$$Y_{12} \cong \omega^2(C_{BD} C_{GB} R_B - C_{GD} C_{GG} R_G) - j\omega C_{GD}$$
$$Y_{21} \cong G_m + \omega^2[C_{GB} R_B(C_{BD} - C_m + C_{ms}) - C_{GG} R_G(C_{GD} + C_m)] - j\omega(C_{GD} + C_m)$$
$$Y_{22} \cong G_{ds} + \omega^2[C_{BD} R_B(C_{BD} - C_m + C_{ms}) + C_{GD} R_G(C_{GD} + C_m)] + j\omega(C_{BD} + C_{GD})$$

📖 H. -C. Han *et al.*, ESSDERC, pp. 269-272, 2022.

RF Extraction Compared to Measurements (RT & CT)

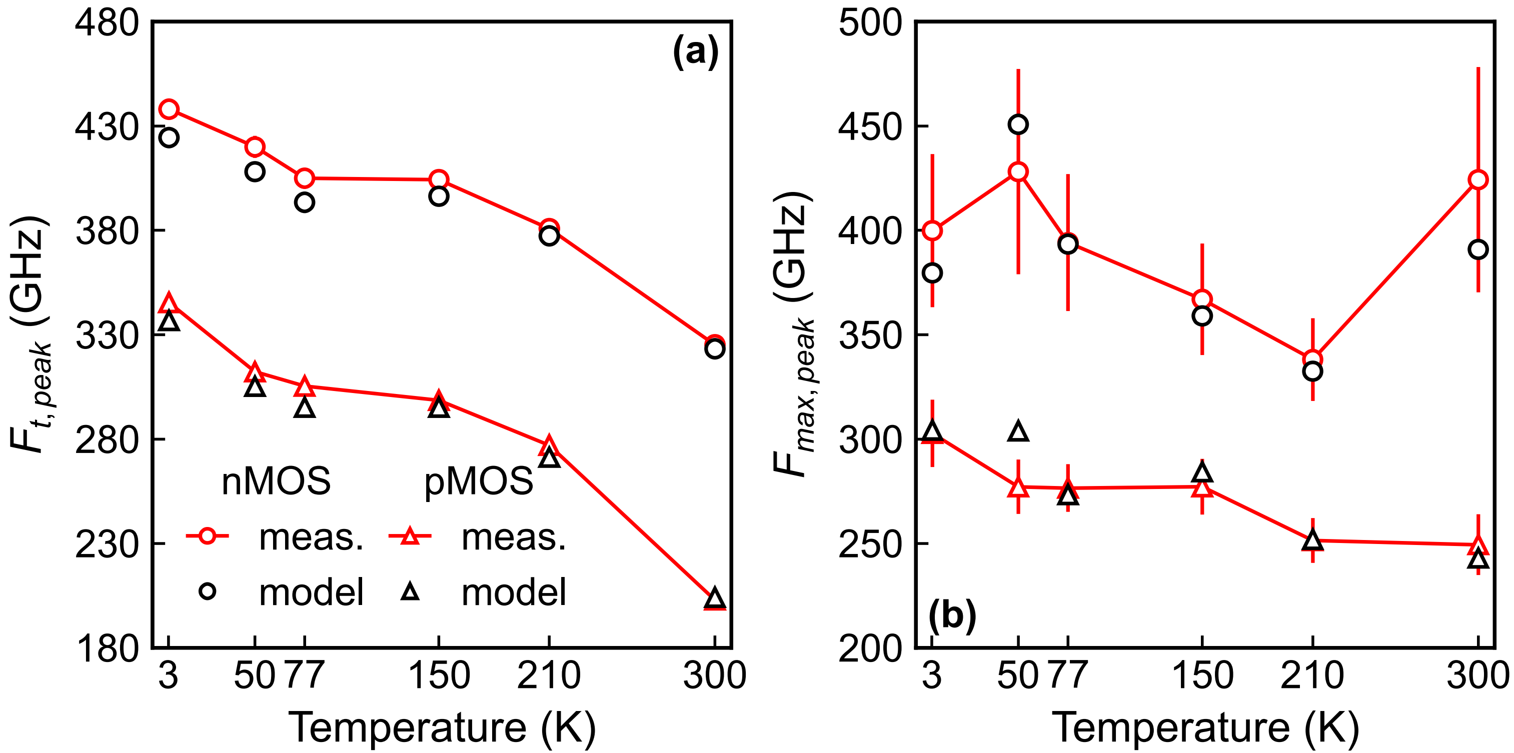


Extracted parameters versus temperature

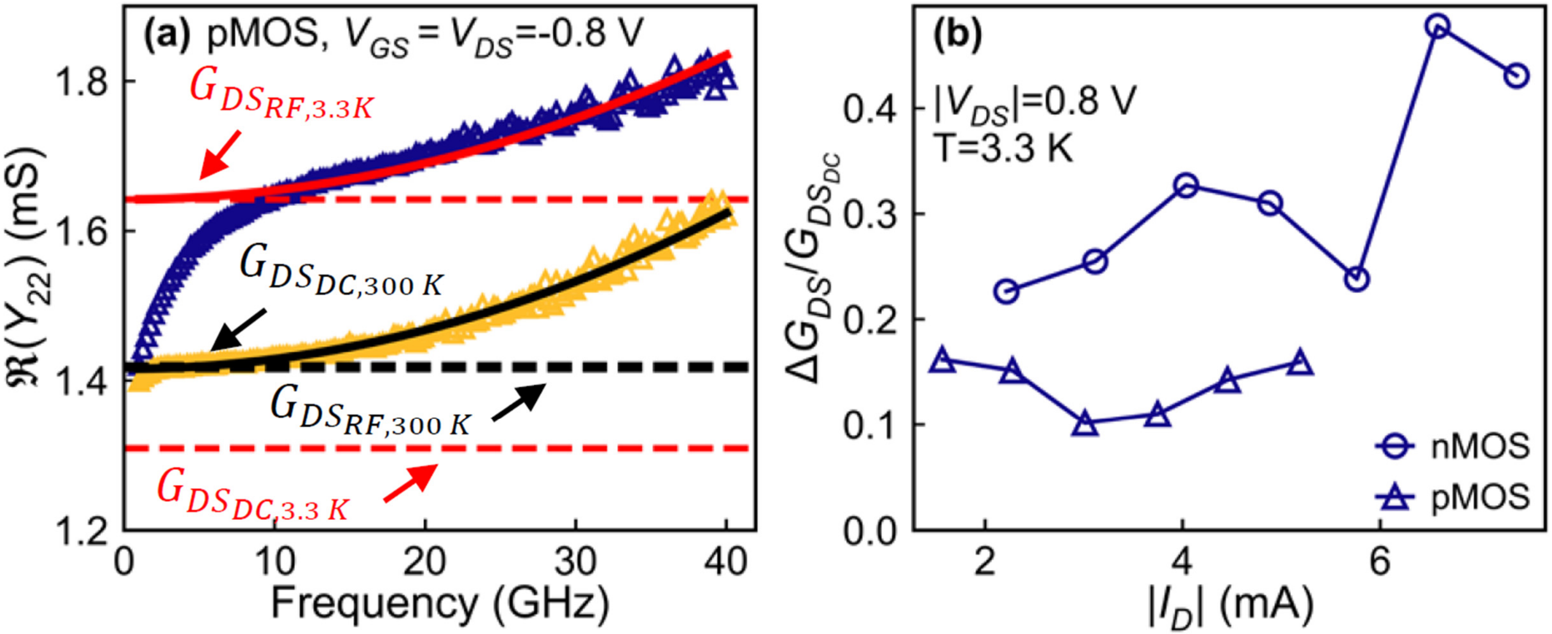


H. -C. Han *et al.*, ESSDERC, pp. 269-272, 2022.

$F_{t,peak}$ and F_{max} versus Temperature



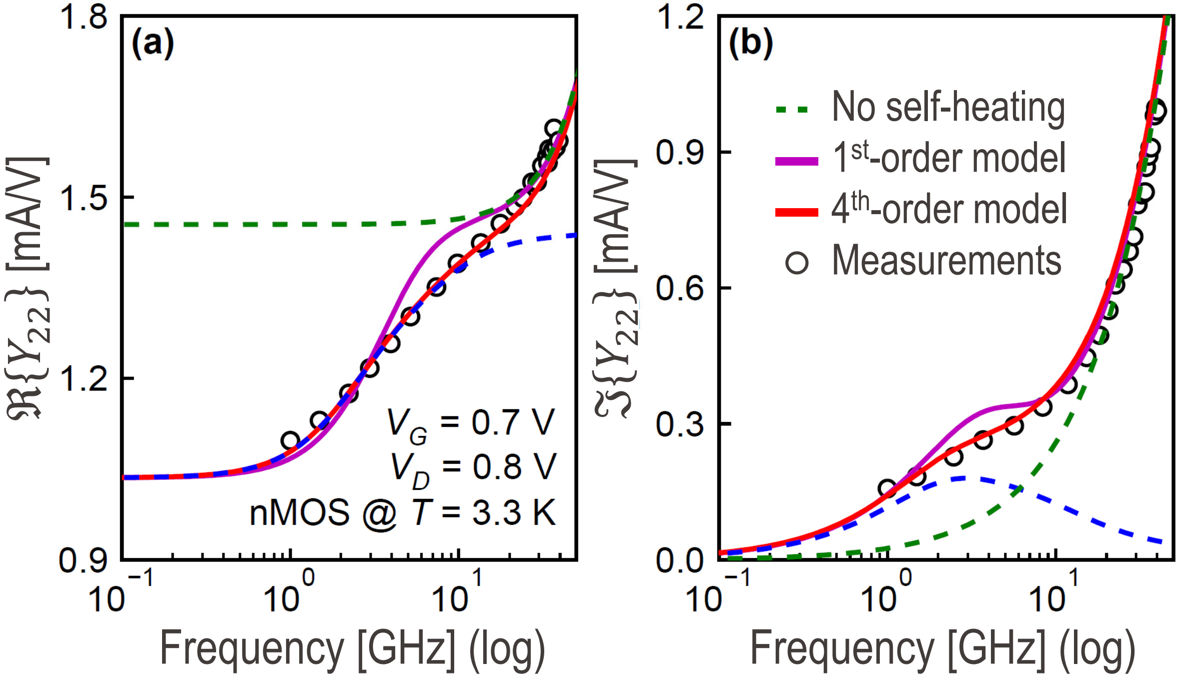
Impact of Self-heating on $\Re(Y_{22})$



- The non-quadratic behavior of $\Re(Y_{22})$ at low frequency is due to **self-heating**
- The difference between $G_{DS_{RF}}$ and $G_{DS_{DC}}$ is due to self-heating and becomes significant at 3.3 K particularly for nMOS

H. -C. Han *et al.*, ESSDERC, pp. 269-272, 2022.

Y-parameters at CT including Self-Heating



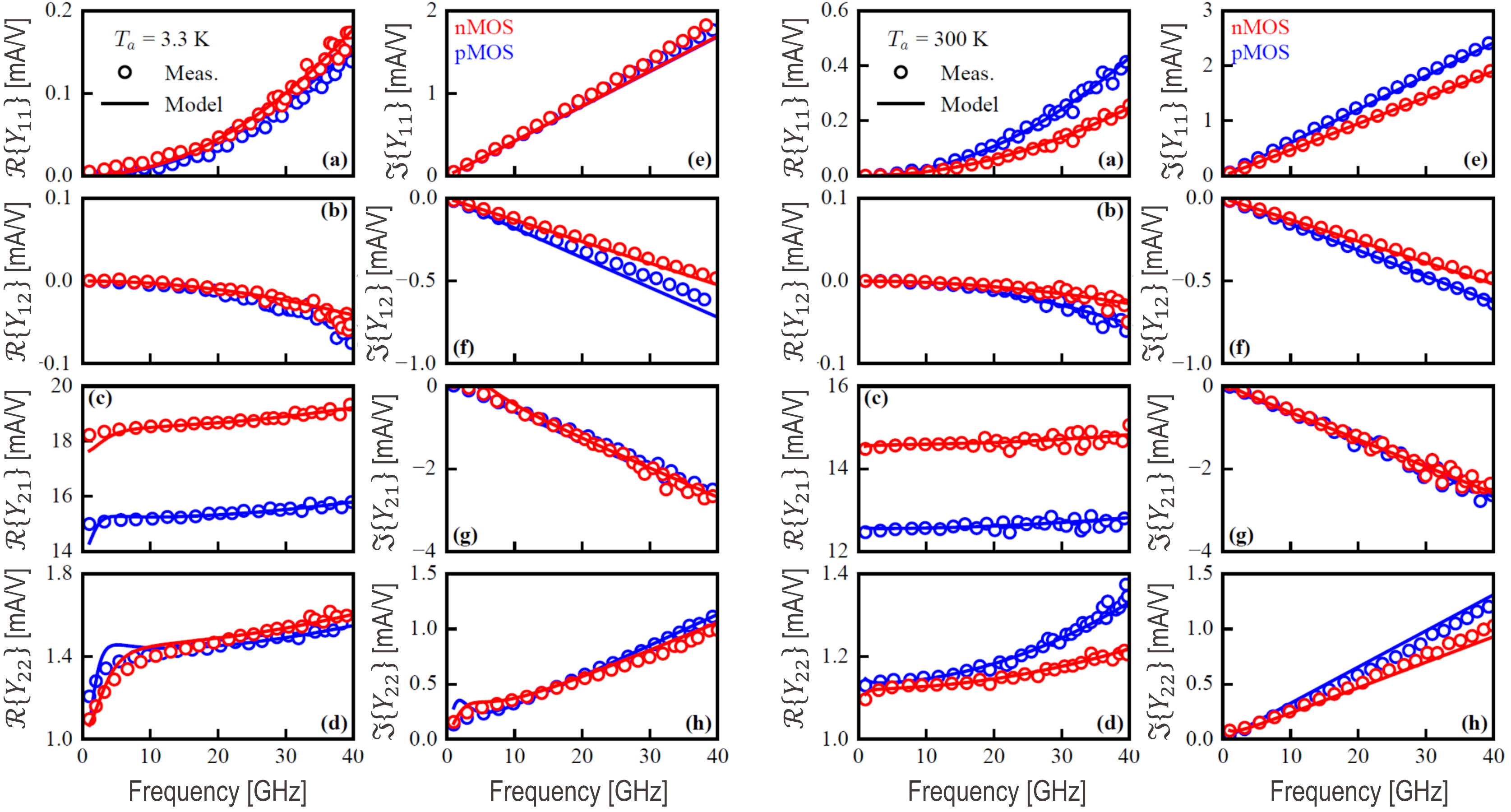
$$Y^{RF} = Y^{NW} + Y^{SH}$$

- Y^{NW} iso-thermal Y-param.
- Y^{SH} dynamic SH term

- A 4th-order thermal network is needed for a proper modeling of the dynamic SH effect

H. -C. Han *et al.*, accepted for publication in JEDS, 2025.

Y-Parameters at RT and CT (incl. SH)



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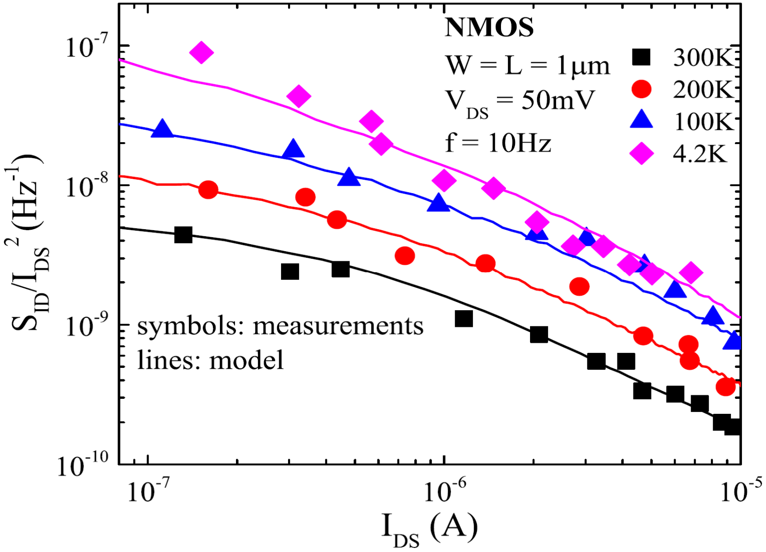
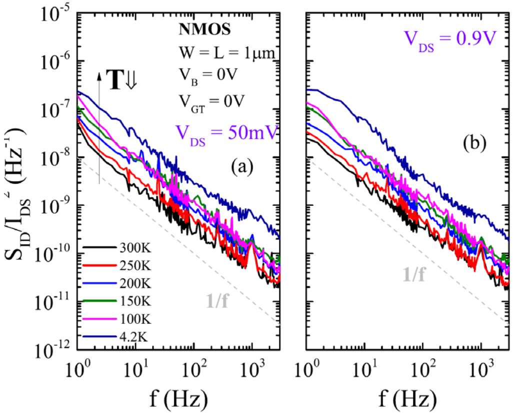
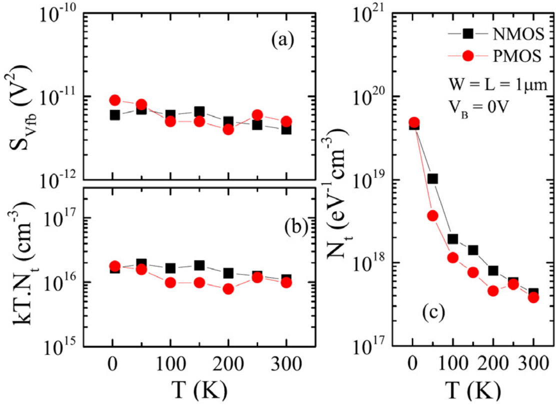
Low-frequency Noise in 22nm FDSOI



$$\frac{S_{ID}}{I_{DS}^2} = \left(\frac{G_m}{I_{DS}}\right)^2 \cdot \left(1 + \Omega \frac{I_{DS}}{G_m}\right)^2 \cdot S_{V_{fb}} \text{ with } S_{V_{fb}} = \frac{q^2 kT\lambda N_t}{WLC_{ox}^2 f}$$





- The noise-to-signal ratio S_{ID}/I_{DS}^2 increases at CT thanks to improved G_m/I_{DS} at CT (in strong inversion)
- The simple model fits the data well down to CT
- Parameter $\Omega \cong 4\ V^{-1}$ and $S_{V_{fb}}$ are almost temperature independent

B. Cardoso Paz , *et al.*, TED, vol. 67, No. 11, Nov. 2020.

White Noise and the Fano Noise Suppression Factor

- The **Fano noise suppression factor** compares the PSD of the drain current fluctuations to the PSD of shot noise which is dominant in weak inversion

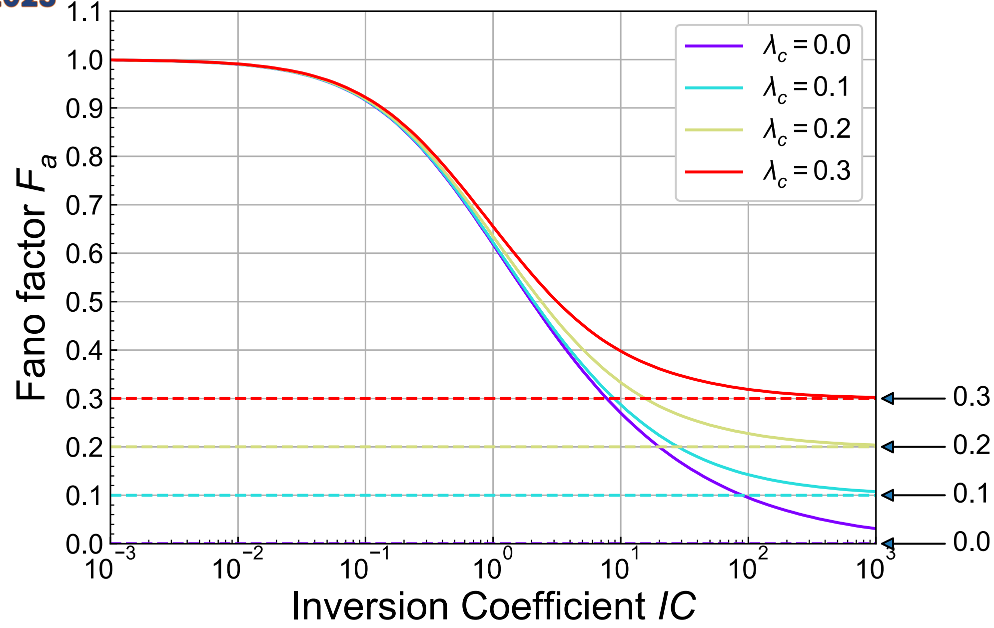
$$F_a = \frac{S_{\Delta I_D^2}}{2qI_D} = \frac{4k_B T \cdot \gamma_n G_m}{2qI_D} = 2U_T \cdot \gamma_n \cdot \frac{G_m}{I_D} = 2\,\frac{\gamma_n}{n} \cdot \frac{g_{ms}(IC)}{IC}$$

- By definition $F_a = 1$ when the noise is **full shot noise** like in weak inversion and $F_a < 1$ when the noise is only **partially** due to shot noise like it is the case in moderate and strong inversion for example
- The Fano noise suppression factor is actually **proportional to the G_m/I_D ratio**
- It can be expressed in terms of the inversion coefficient IC by using the **normalized** G_m/I_D ratio

$$\frac{g_{ms}(IC)}{IC} = \frac{G_m\, nU_T}{I_D} = \frac{\sqrt{4IC + 1 + (\lambda_c IC)^2} - 1}{IC\,(2 + \lambda_c^2 IC)}$$

C. C. Enz and H.-C. Han, "The Fano Noise Suppression Factor and the G_m/I_D FoM," ISCAS 2023.

The Fano Factor versus IC for Short Channel Transistors



- For short-channel

$$F_a \cong (1 + \lambda_c^2 \cdot IC) \cdot \frac{g_{ms}(IC)}{IC}$$

- where $\lambda_c \triangleq \frac{L_{sat}}{L}$
- with $L_{sat} = \frac{2\mu_0 \cdot U_T}{v_{sat}} = \frac{2U_T}{E_c}$
- In strong inversion

$$F_a \cong \lambda_c$$

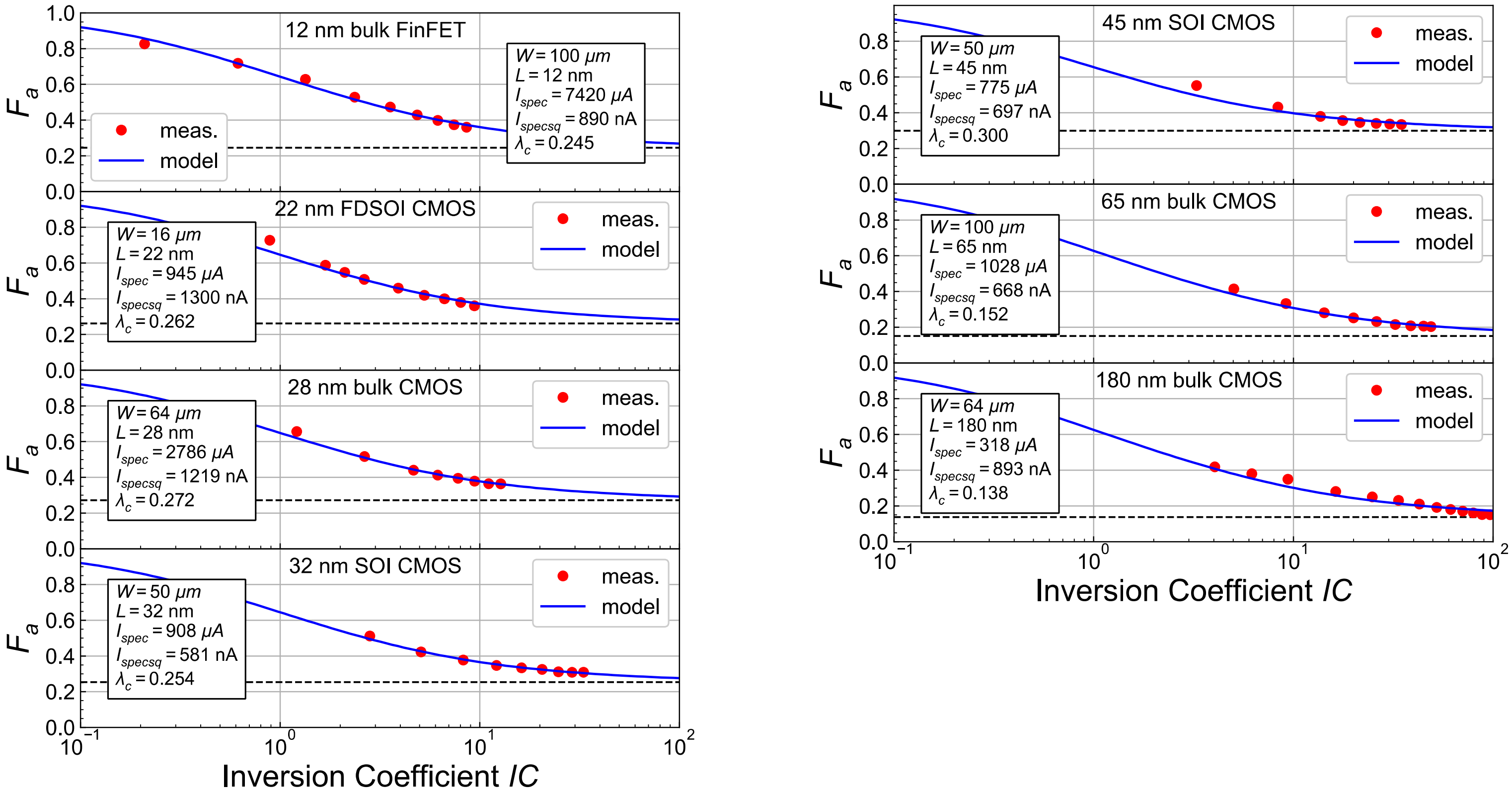
- In weak inversion

$$F_a \cong 1$$

- The Fano noise suppression factor is limited to λ_c in strong inversion

C. C. Enz and H.-C. Han, "The Fano Noise Suppression Factor and the G_m/I_D FoM," ISCAS 2023.

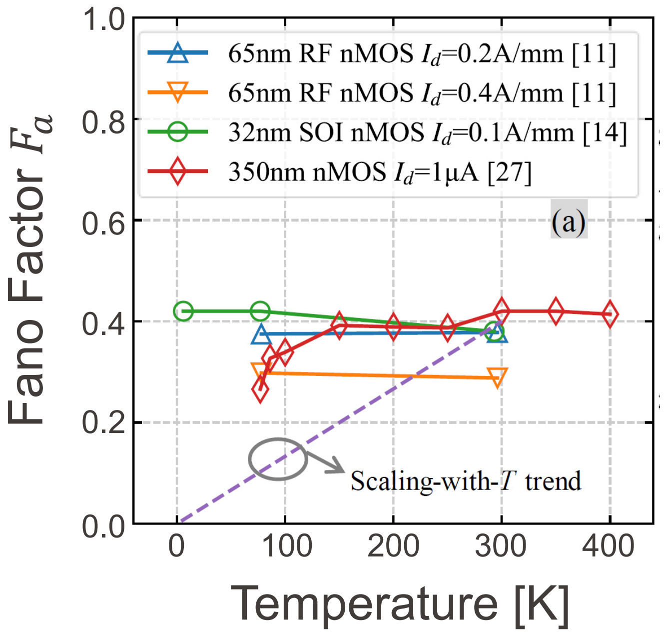
Fano Factor Measured on Several Technologies (RT)

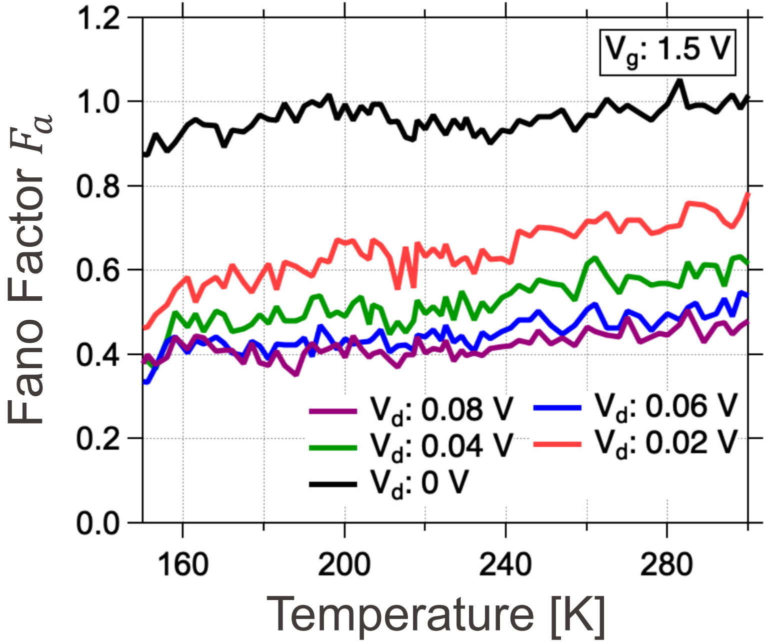


C. Enz and H.-C. Han, ISCAS 2023.

S. Das and J. C. Bardin, "Characterization of Shot Noise Suppression in Nanometer MOSFETs," IMS, June 2021, pp. 892–895.

Fano Suppression Factor F_a versus Temperature





- Like the normalized G_m/I_D, the Fano noise suppression factor F_a is almost **temperature independent**, but depends on the inversion coefficient IC

📖 K. Ohmori and S. Amakawa, JEDS, vol. 9, Sept. 2021.
📖 X. Chen, H. Elgabra, C.-H. Chen, J. Baugh, L. Wei, ISCAS 2021.

Outline

- Introduction
- Subthreshold current and swing
- Threshold voltage
- Simplified EKV model at CT
- RF modeling
- Noise modeling
- **Conclusion**

Conclusion

- Available CMs do not scale correctly with T down to CT
- Most MOSFET DC features improve at CT except
  - V_{T0} which increases
  - SS which saturates
  - Additional hopping and tunneling subthreshold currents appear for short-channel at high V_{DS} voltage
- The sEKV can do a good job modeling silicon devices at CT
- RF Y-parameters can be properly modelled at CT, but self-heating needs to be accounted for in $\Re(Y_{22})$
- The white noise can be modelled with the Fano noise suppression factor taking advantage of the temperature independence of the normalized G_m/I_D FoM

Additional Resources

- Github page of Christian Enz:

  https://github.com/chrisenz

- General analog circuit design:

  https://github.com/chrisenz/Analog-Circuit-Design

- Currently including:
  - Optimization of capacitive closed loop CS amplifier
  - AC simulation of SC circuits with a standard Spice simulator
  - And many more to come…

EPFL

Thank you

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